DC/DC Digital Controller with PMBus Interface

Hynetek Semiconductor Co., Ltd.

HP1000A

FEATURES

- Versatile Digital Voltage Mode Controller
- −40°C to +125°C Operating Temperature
- PMBus Revision 1.2 Compliant with PEC and Extended Manufacturer Specific Commands
- 6 PWM Control Signals with 312.5 ps Resolution
  - Programmable Switching Frequency from 48.8 kHz to 1 MHz
  - Multi-segments Soft-start of Duty and Switching Period for Open-loop LLC
  - Frequency Synchronization
  - Suport HiZ Mode
  - Active Snubber Control
- High-speed Voltage Sense
  - Independent 50 MHz 11-bit Tracking ADC for Input Voltage and Output Voltage Sense
  - Up to 1.6 V Differential Input Voltage Range
  - Secondary-side Rectified Voltage Sense Capability for VFF
- High-speed Current Sense
  - Independent 25 MHz Σ-Δ ADC for Primary-side and Secondary-side Current Sense
  - Primary-side Cycle-by-cycle Fast OCP
  - Secondary-side Cycle-by-cycle Fast OCP
  - Secondary-side Diode Emulation Mode
- Advanced Control Algorithm
  - Digital Control Loop with Programmable Loop Filters
  - Duty-cycle Double Update
  - Fast Line Voltage Feed-forward
  - Pre-bias Startup
- Auxiliary Functions
  - Accurate Droop Current Sharing and Active Current Sharing
  - Constant Current Loop
  - Compatible with NTC and DrMOS Temperature Sense
  - Programmable Output Voltage Redundant OVP
  - Extensive Fault Detection and Protection
  - Low-power Mode During PSU Off
  - Analog Interleaved Phase Delay Setting
  - Timed Output Current Protection
  - Compatible with DOSA Analog Trim
  - Up to 4 GPIOs
- Programming Via Easy-to-use Graphical User Interface (GUI)
- 512 Bytes EEPROM for Programming and Data Storage
- Available at 4 mm x 4 mm QFN-24L Packages

APPLICATIONS

Intermediate Bus Converters (IBC)
Isolated DC/DC Power Supplies and Modules
Industrial 4.0 Power Applications

GENERAL DESCRIPTION

The HP1000A is a versatile digital controller designed for high-density, high-efficiency DC-DC power conversion, with PMBus™ Revision 1.2 compliant interface. This device provides advanced power control solutions targeted at isolated and non-isolated DC-DC secondary-side applications, including full-bridge/half-bridge isolated converters, open-loop LLC converters, multi-phase buck converters, etc.

The HP1000A offers extensive programmability of integrated digital compensators, fast input line feed-forward, PWM output types and timing, constant current mode, as well as soft-start/stop sequences and synchronization. Additionally, it provides flexible protection features including over-voltage protection (OVP), short-circuit protection (SCP), reverse current protection (RCP), over-temperature protection (OTP), and ensuring a robust power management solution.

The HP1000A employs a flexible state machine architecture programmed via intuitive GUI. This user-friendly interface reduces design cycle time while producing a robust, hardware-coded system embedded in the built-in EEPROM.

The HP1000A is available in 4 mm x 4 mm QFN-24L.

TYPICAL APPLICATION CIRCUIT

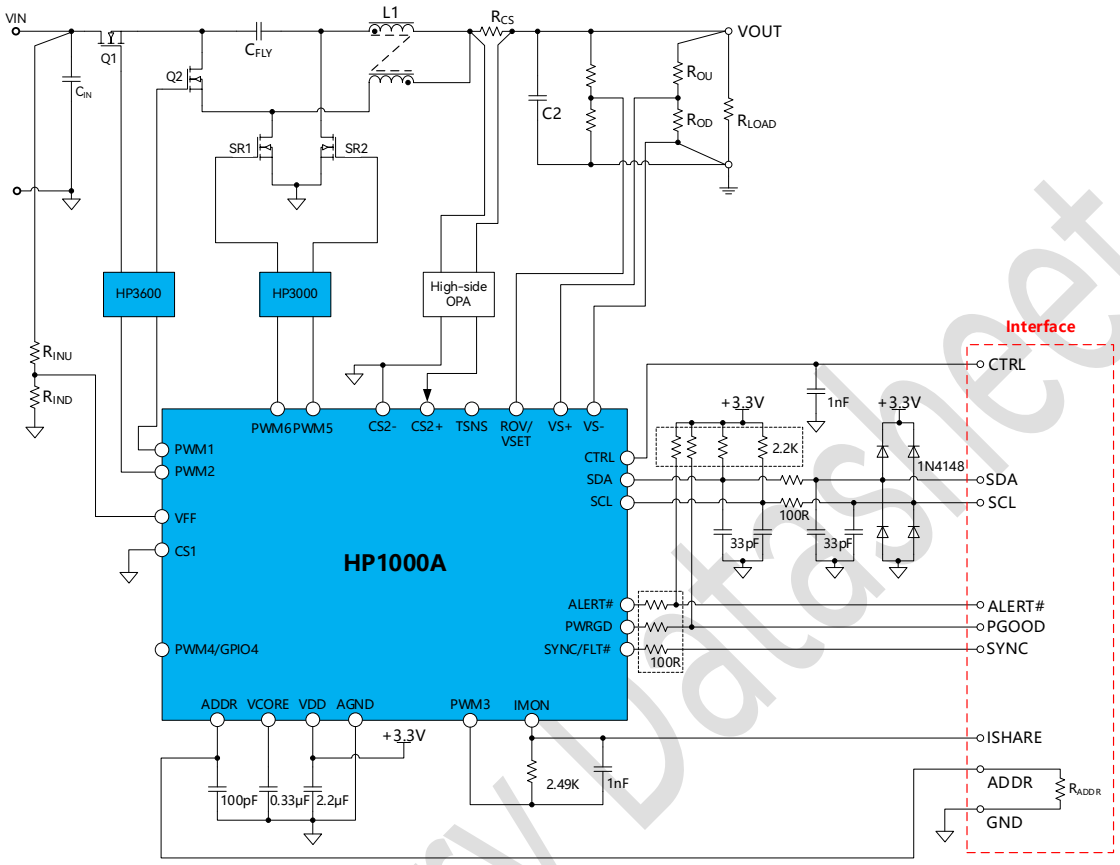

Figure 1. Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 0.1	03/2026	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

HP1000A-AA001-QN24R

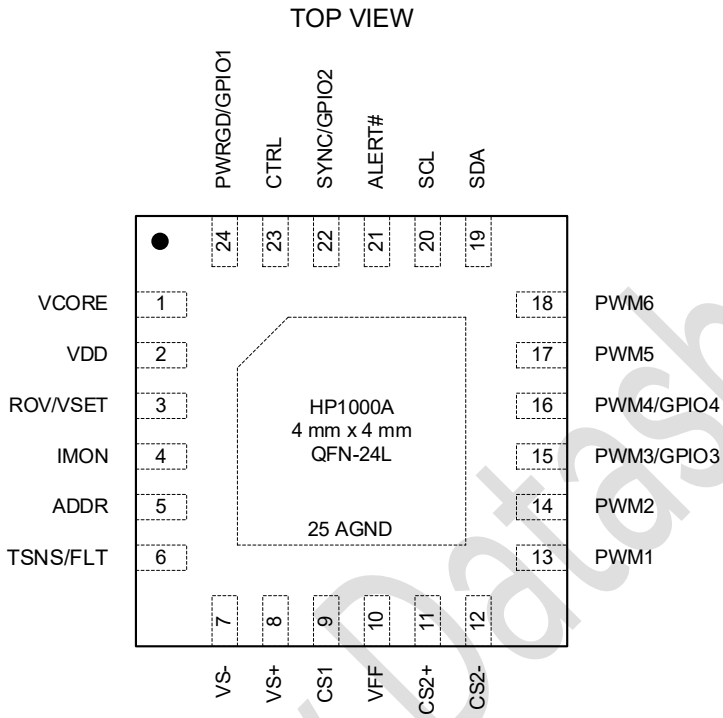


Figure 2. HP1000A-AA001-QN24R Pin Assignment

Table 1. Pin Function Description of HP1000A-AA001-QN24R

Pin No.	Pin Name	Type[1]	Description
1	VCORE	P	**Output of 1.8 V Regulator.** Connect a decoupling capacitor of at least 330 nF from this pin to AGND, as close as possible to VCORE, minimizing the PCB trace length.
2	VDD	P	**Power Supply Input.** Voltage of 3.0 V to 3.6 V. This signal is referenced to AGND. Connect a 2.2 µF decoupling capacitor from this pin to the AGND, as close as possible to minimize the PCB trace length.
3	ROV/VSET	AI	**Redundant Over-Voltage Protection** This signal is referenced to VS−. This pin can be reused as DOSA analog trim. This pin can be reused as primary voltage sense for pre-bias startup.
4	IMON	AIO	**Output Current Indicator.** The IMON pin outputs a DAC current source proportional to the sensed total average current from CS2 pins.
5	ADDR	AI	**PMBus/I²C Address Setting.** Connect a resistor between the ADDR pin and AGND. This signal is referenced to AGND.
6	TSNS	AI	**Thermistor Input.** It is capable with NTC resistor temperature sense signal. This pin is referenced to AGND. Connect this pin to AGND if not in use.
7	VS-	AI	**Differential Voltage Sense, Negative Input.** This is the connection for the ground line of the power rail. Provide a low ohmic connection to AGND.
8	VS+	AI	**Differential Voltage Sense, Positive Input.** This signal is referenced to VS−.

1 Legend:

A = Analog Pin

P = Power Pin

D = Digital Pin

I = Input Pin

O = Output Pin

Pin No.	Pin Name	Type[1]	Description
9	CS1	AI	**Current Sense 1 Input.** This pin is connected to the primary side current sensing ADC and to the cycle-by-cycle current-limit comparator. This signal is referenced to AGND. Connect this pin to AGND if not in use.
10	VFF	AI	**VIN Voltage Sense.** This pin can be utilized as primary side input voltage sensing, fast input voltage feed-forward, pre-bias start-up, and input voltage UVLO protection. This signal is referenced to AGND.
11	CS2+	AI	**Non-inverting Differential Current Sense 2 Input.** This signal is referenced to CS2−. If this pin is not used, connect it to AGND.
12	CS2-	AI	**Inverting Differential Current Sense 2 Input.** If this pin is not used, connect it to AGND. This pin must have a low ohmic connection to AGND though the sense resistor.
13	PWM1	DO	**PWM1 Output.** This pin can be disabled when not in use. This signal is referenced to AGND.
14	PWM2	DO	**PWM2 Output.** This pin can be disabled when not in use. This signal is referenced to AGND.
15	PWM3	DO	**PWM3 Output.** This pin can be disabled when not in use. This signal is referenced to AGND. This pin can also be programmed as a GPIO3.
16	PWM4	DO	**PWM4 Output.** This pin can be disabled when not in use. This signal is referenced to AGND. This pin can also be programmed as a GPIO4.
17	PWM5	DO	**PWM5 Output.** This pin can be disabled when not in use. This signal is referenced to AGND. This pin can also be programmed as a GPIO5.
18	PWM6	DO	**PWM6 Output.** This pin can be disabled when not in use. This signal is referenced to AGND. This pin can be used as active current sharing control.
19	SDA	DIO	**PMBus/I²C Serial Data Input and Output (Open Drain).** This signal is referenced to AGND.
20	SCL	DIO	**PMBus/I²C Serial Clock Input (Open Drain).** This signal is referenced to AGND.
21	ALERT#	DO	**SMBus ALERT#.** Connect this pin to VDD through a pull-up resistor (typically 2.2 kΩ). This signal is referenced to AGND.
22	SYNC	DIO	**Frequency Synchronization.** Connect this pin to AGND if not in use. This pin can also be programmed as GPIO2.
23	CTRL	DIO	**Control Input.** It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for noise debounce and decoupling. This signal is referenced to AGND.
24	PWRGD	DO	**POWER GOOD Output (Open Drain).** Connect this pin to AGND if not in use. This pin can also be programmed as GPIO1.
E-PAD	AGND	P	**Exposed Pad for Ground.** For increased reliability of the solder joints and maximum thermal capability, the exposed pad should be soldered to the PCB AGND plane.

SPECIFICATIONS

V_{DD} = 3.0 to 3.6 V, T_A = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3.0	3.3	3.6	V
Supply Current	I_{DDQ}	Power off (CTRL shut-down, or OPERATION = off)		1.5		mA
Supply Current	I_{DD}	Normal operation: PWM pins unloaded		18	22.5	mA
		During EEPROM programming		I_{DD} + 6		mA
		Shutdown; V_{DD} below undervoltage lockout (UVLO)		50	100	µA
POWER-ON RESET						
Power-On Reset		V_{DD} rising	2.7	2.8	2.9	V
UVLO Threshold		V_{DD} falling	2.55	2.65	2.75	V
UVLO Hysteresis				150		mV
OVLO Threshold			3.7	3.9	4.1	V
OVLO Debounce		V_{DD_OV} flag debounce set to 2 µs		2		µs
		V_{DD_OV} flag debounce set to 500 µs		500		µs
VCORE PIN						
Output Voltage	V_{CORE}	330 nF capacitor connected to AGND	1.7	1.8	1.9	V
OVLO Threshold			2.0	2.1	2.2	V
OVLO Debounce		V_{CORE_OV} flag debounce set to 2 µs		2		µs
		V_{CORE_OV} flag debounce set to 500 µs		500		µs
OSCILLATOR AND PLL						
PLL Frequency			190	200	210	MHz
Digital PWM Resolution				312.5		ps
PWM1 to PWM6 PINS						
Output Low Voltage	V_{OL}	I_{OH} = +10 mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −10 mA	V_{DD} − 0.8			V
Rise Time	t_R	C_{LOAD} = 50 pF		4	6	ns
Fall Time	t_F			4	6	ns
Output Source Current	I_{OL}		−10			mA
Output Sink Current	I_{OH}				10	mA
Leakage Current	I_{OZ}				1	µA
VS+, VS− VOLTAGE SENSE PINS						
Voltage Sense ADC						
Input Differential Voltage Range	V_{OUT}	Differential voltage from VS+ to VS−	0		1.6	V
Error Voltage Digital Resolution				11		bits
Input Impedance				1		MΩ
Sample Rate			0	50		MHz
Measurement Resolution		1.0 V to 1.6 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ	-1	±0.75	1	%
		0.8 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ	-1.4	±1.0	1.4	%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		0.2 V to 0.4 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ		±10.5		mV
Fast OVP Comparator		Triggers VOUT_OV_FAULT flag				
OVP Voltage Range		Differential voltage from OVP to VS−	0.80		1.6	V
OVP DAC Resolution				6		Bit
Threshold Accuracy		0.80 V to 1.6 V voltage range	−2.0		+2.0	%
		Trimmed at 1.206 V	-1.0		+1.0	%
Hysteresis				20		mV
Propagation Delay (Latency)		Debounce time not included		60	100	ns
ROV/VSET PIN						
Fast ROV Comparator						
OVP Voltage Range		Differential voltage from OVP to VS−	0.80		1.6	V
OVP DAC Resolution				6		Bit
Threshold Accuracy		0.8 V to 1.6 V voltage range	−2.0		+2.0	%
		Trimmed at 1.206 V	-1.0		+1.0	%
Hysteresis				20		mV
Propagation Delay (Latency)		Debounce time not included		60	100	ns
VSET ADC						
Valid Input Voltage Range			0		1.6	V
ADC Clock Frequency				25		MHz
Register Update Rate				10		ms
Measurement Resolution				12		Bits
Measurement Accuracy		10% to 90% of the input voltage range	-1		+1	%
Leakage Current					1.0	µA
VFF VOLTAGE SENSE PIN						
VFF ADC						
Input Voltage Range	V_{FF}	Input voltage from VFF to AGND	0		1.6	V
Error Voltage Digital Resolution				11		bits
Input Impedance				1		MΩ
Sample Rate			0	50		MHz
Measurement Resolution		1.0 V to 1.6 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ	-1	±0.75	1	%
		0.8 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ	-1.4	±1.0	1.4	%
		0.2 V to 0.4 V, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3σ		±10.5		mV
Edge Comparator						
Hysteresis				23		mV
Propagation Delay (Latency)		Debounce time not included		15		ns
Digital De-glitcher Resolution				5		ns
Edge Detection Threshold Accuracy		When set to 300 mV	270	300	330	mV
		When set to 500 mV	450	500	550	mV
CS1 CURRENT SENSE PIN						
CS1 ADC						
Input Voltage Range			0		1.6	V
ADC Clock Frequency				25		MHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Register Update Rate				25		kHz
Measurement Resolution				10		Bits
Current Sense Measurement Accuracy		Factory trimmed at 1.0 V; tested under dc input conditions				
		10% to 90% of usable input voltage range	−2.0		+2.0	%
CS1 Fast OCP Comparator		Triggers internal CS1_OCP flag				
Threshold Accuracy		When set to 1.2 V (Trim set point)	1.17	1.2	1.23	V
		When set to 0.25 V	0.23	0.25	0.27	V
Hysteresis				20		mV
Propagation Delay (Latency)		Debounce/blanking time not included		40	80	ns
Leakage Current					1.5	µA
CS2+, CS2− CURRENT SENSE PINS						
Current Sense ADC						
ADC Clock Frequency				25		MHz
Register Update Rate				25		kHz
Measurement Resolution				10		Bits
Current Measurement Sense Accuracy						
30 mV Setting		10% to 90% of the input voltage range	−3		+3	%
60 mV Setting		10% to 90% of the input voltage range	−1.5		+1.5	%
240 mV Setting		10% to 90% of the input voltage range	−1		1	%
CS2 CBC Comparator		For CS2 fast OCP and peak constant current mode				
Threshold Resolution				6		Bit
Threshold Range of 360 mV						
Threshold Accuracy		Trimmed at 240 mV	-2		2	%
		Threshold set at 91.4 mV (16 LSB)	-4		4	%
		Threshold set at 274.3 mV (48 LSB)	-4		4	%
Hysteresis				20		mV
Propagation Delay (Latency)		Debounce time not included		60	100	ns
Threshold Range of 90 mV						
Accuracy		Trimmed at 60 mV	-3		3	%
		Threshold set at 22.85 mV (16 LSB)	-5		5	%
		Threshold set at 68.5 mV (48 LSB)	-5		5	%
Hysteresis				4		mV
Propagation Delay (Latency)		Debounce time not included		60	100	ns
CS2 ZCD Comparator						
Threshold Resolution				7		Bit
Threshold Range		Offset binary coding. 0 mV = 64 LSB				
Threshold Accuracy		Trimmed at 7.5 mV	-2		2	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		Threshold set at -30 mV (0 LSB)	-3		3	mV
		Threshold set at -15 mV (32 LSB)	-2		2	mV
		Threshold set at 0 mV (64 LSB)	-2		2	mV
		Threshold set at 15 mV (96 LSB)	-2		2	mV
		Threshold set at 29.53 mV (127 LSB)	-3		3	mV
Hysteresis				2.4		mV
Propagation Delay (Latency)		Debounce time not included		80	110	ns
TSNS/FLT PIN						
Internal Source Current			44.6	46	47.3	µA
TSNS ADC						
ADC Clock Frequency				25		MHz
Register Update Rate				10		ms
Measurement Resolution				12		Bits
Input Voltage Range for NTC			0		1.6	V
Measurement Accuracy		10% to 90% of the input voltage range, NTC mode	−1		+1	%
Input Voltage Range for DrMOS			0		2.0	V
Measurement Accuracy		10% to 90% of the input voltage range, DrMOS mode	−1		+1	%
Fault Detection						
DAC Threshold			0.65		2.4	V
Resolution				3		bit
LSB				0.25		V
Threshold Accuracy		Trimmed at 2.0 V	-5		5	%
Hysteresis				20		mV
Propagation Delay (Latency)		Debounce/blanking time not included		40	80	ns
Negative Temperature Sense Through Junction		Threshold = 0°C	-4		4	°C
IMON PIN						
IMON Current DAC						
Output Current Range	I_{MON_DAC}		0		640	µA
Output Current Resolution		6-bit + 1-bit modulation		10		µA
Output Current Accuracy		Trimmed at I_{MON_DAC} = 320 µA	-1%		1%	
		10% to 90% of the usable range	-2%		2%	
DAC Update Rate				1		MHz
IMON ADC						
Valid Input Voltage Range			0		1.6	V
ADC Clock Frequency				25		MHz
Register Update Rate				10		ms
Measurement Resolution				12		Bits
Measurement Accuracy		10% to 90% of the input voltage range	-1.5		1.5	%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CTRL, PWRGD, GPIO1 to GPIO4 PINS						
Input Low Level	V_{IL}				0.8	V
Input High Level	V_{IH}		V_{DD} − 0.8			V
Output Low Level	V_{OL}	Sink current = 10 mA			0.4	V
Output High Level	V_{OH}	Sink current = -10 mA	V_{DD} − 0.8			
Leakage Current					1.0	µA
SYNC PIN						
Input Low Level	V_{IL}				0.4	V
Input High Level	V_{IH}		V_{DD} − 0.8			V
Operating As Sync slave (SYNI)		Synchronization to external frequency				
Synchronization Range % of Internal Clock Period	t_{SYNC}		90		110	% F_{SW}
SYNI Positive Pulse Width		External clock applied on SYNI pin	360			ns
SYNI Negative Pulse Width		External clock applied on SYNI pin	360			ns
SYNI Period Drift		Period drift between two consecutive external clocks			280	ns
Operating As Sync Master (SYNO)						
Positive Pulse Width			600	640	680	ns
Output Low Level	V_{OL}	Sink current = 10 mA			0.4	V
Output High Level	V_{OH}	Sink current = -10 mA	V_{DD} − 0.8			
Leakage Current					1.0	µA
SDA, SCL, ALERT# PINS						
Input Voltage Low	V_{IL}				0.8	V
Input Voltage High	V_{IH}		V_{DD} − 0.8			V
Output Low Level	V_{OL}	Sink current = 10 mA			0.4	V
Leakage Current			−1		+1	µA
ADDR PIN						
Internal Current Source	I_{ADDR}		8.21	8.5	8.79	µA
SERIAL BUS TIMING						
Clock Operating Frequency			10	100	400	kHz
Glitch Immunity					50	ns
Bus Free Time	t_{BUF}	Between stop and start conditions	1.3			µs
Start Setup Time	t_{SU_STA}	Repeated start condition setup time	0.6			µs
Start Hold Time	t_{HD_STA}	Hold time after (repeated) start condition; after this period, the first clock is generated	0.6			µs
Stop Setup Time	t_{SU_STO}		0.6			µs
SDA Setup Time	t_{SU_DAT}		100			ns
SDA Hold Time	t_{HD_DAT}	For read-back	125			ns
		For write	300			ns
SCL Low Timeout	$t_{TIMEOUT}$		25		35	ms
SCL Low Time	t_{LOW}		0.6			µs
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Extend Time	t_{LOW_SEXT}				25	ms
SCL, SDA Rise Time	t_R		20		300	ns
SCL, SDA Fall Time	t_F		20		300	ns
EEPROM						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EEPROM Update Time		Time from the update command to completion of the EEPROM update			40	ms
Reliability						
Endurance		T_J = 85 °C	10,000			Cycles
		T_J = 125 °C	1000			Cycles
Data Retention		T_J = 85 °C	20			Years
		T_J = 125 °C	15			Years

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDD (Continuous) to AGND	4.2 V
VCORE to AGND	2 V
VFF, IMON, ADDR, TSNS/FLT, VS+, OVP, CS1, CS2+, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, SDA, SCL, ALERT#, SYNC, CTRL, PWRGD to AGND	-0.3 V to V_{DD} + 0.3 V
VS-, CS2- to AGND	-0.3 V to +0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	±6000 V
Charge Device Model	±1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN-24L	TBD	TBD	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

OVERVIEW

The HP1000A is an advanced digital power controller engineered for high-performance DC-DC conversion in demanding industrial and telecommunications environments. Designed to operate across a wide temperature range of -40°C to +125°C, it combines precision sensing, adaptive control algorithms, and robust programmability to optimize efficiency and reliability. Leveraging a 50 MHz tracking ADC and 25 MHz Σ-Δ ADC, the controller achieves exceptional accuracy in voltage regulation (0.78125 mV/LSB resolution) and current monitoring, ensuring stable operation across diverse topologies such as hard-switching full-bridge, buck, open-loop LLC resonant converters, and push-pull configurations. Its 6 programmable PWM outputs, with 312.5 ps resolution, enable precise timing control for both primary-side switches and synchronous rectifiers, while light-load efficiency modes minimize power losses.

The HP1000A excels in system integration through its PMBus Revision 1.2 compliant interface, allowing real-time configuration and monitoring of critical parameters like voltage, current, and temperature. Four flexible GPIOs expand functionality, supporting features such as active clamp snubber control, external fault signal detection, or synchronization with external clocks. Comprehensive protection mechanisms, including cycle-by-cycle over-current limits, redundant over-voltage detection, and short-circuit protections, enhance system resilience. Additionally, its active current-sharing capabilities simplify parallel operation in high-power applications.

Targeting applications in telecom infrastructure, server motherboards, and industrial power systems, the HP1000A is offered in compact 4×4 mm QFN-24L package, minimizing PCB footprint. Supported by an intuitive GUI and onboard EEPROM for standalone operation, it accelerates design cycles and ensures adaptability to evolving power requirements. By balancing high-speed digital control with analog precision, the HP1000A stands as a versatile solution for next-generation power architectures demanding efficiency, scalability, and robustness.

VDD AND VCORE

When the voltage of the VDD pin is applied (VDD), there is a delay before the part can regulate the power supply. When VDD rises above the power-on reset and UVLO levels, it takes ~20 µs for the VCORE pin (Pin 1) to reach its operational point of 2.8 V (Typical). The EEPROM contents are then downloaded to the registers. The download takes approximately an additional 1.2 ms. After the EEPROM contents are downloaded, the HP1000A is ready for operation; however, it takes a maximum of ~2 ms for the HP1000A to complete initialization of the address after a power-on reset. Therefore, it is recommended that the master device access the HP1000A at least 5 ms after power-on reset.

If the HP1000A is programmed to power up at this time, the soft start ramp begins. Otherwise, the part waits for a PSON signal, as programmed in Register 0x01 and Register 0x02.

To minimize trace length, the proper amount of decoupling capacitance must be placed between the VDD pin (Pin 2) and the AGND pin (Expand Pad Pin 25), as close as possible to the device. The same requirement applies to the VCORE pin (Pin 1). It is recommended that the VCORE pin is not used as a reference or to generate other logic levels using resistive dividers.

VOLTAGE SENSE

Tracking ADC

The HP1000A integrates two dedicated high-speed voltage analog-to-digital converters (ADCs). These ADCs are allocated to two critical sensing functions: output voltage sensing (VS) and input voltage sensing (VFF). The VFF channel specifically enables rectified voltage sensing in isolated topologies such as full-bridge converters, leveraging secondary-side rectified voltage measurements for high-speed feed-forward control. Both ADCs deliver 11-bit resolution with an LSB size of 0.78125 mV, covering a full-scale range of 0 to 1.6 V.

Output Voltage Sense

The VS+ (Pin 5) and VS− (Pin 6) pins of the HP1000A are used for the monitoring, control, and protection of the power supply output. Typically, the power rail's VS sense point (typically connected to the output stage) must be connected through an external resistor divider (R_{OU} and R_{DU} in Figure 1) to maintain a nominal 1V differential signal. This scaling is critical because the HP1000A's VS differential ADC accepts only 0 to 1.6V full-scale range. The READ_VOUT (0x8B) command reports the average output voltage; this reading is updated every 10.5 ms.

The VOUT_SCALE_ MONITOR command (Register 0x2A) is programmed for correct output voltage reading.

Input Voltage Sense

The input voltage is monitored through the VFF pin (Pin 10), which can be configured to directly measure the primary-side input voltage (Vin). When configured for direct sensing, the VFF ADC provides a continuous output signal, avoiding the pulsating behavior seen in rectified voltage (V_{RECT}) measurements. The ADC supports an input range of 0 to 1.6 V, enabling precise monitoring of the input voltage. This mode is ideal for applications requiring stable, real-time input voltage tracking for non-isolated applications.

When sensing rectified voltage (V_{RECT}), the VFF pin captures pulsating signals synchronized with the primary-side PWM rising edge. To mitigate noise and ringing in bridge topologies, the measurement cycle is controlled by VFF settings. A programmable deglitcher filters spurious edges, ensuring accurate sampling. If enabled, the deglitcher delays the comparator output, requiring adjustment of the tracking start timer to maintain timing integrity. This method is critical for topologies like phase-shift full-bridge, where V_{RECT} pulses must be sampled during stable intervals.

CURRENT SENSE

The HP1000A integrates two current-sense inputs: CS1 (Pin 9) for primary-side input current monitoring and CS2± (Pins 11/12) for secondary-side differential output current sensing, both leveraging 25 MHz Σ-Δ ADCs with 1-bit native resolution enhanced to high effective resolution through oversampling and noise-shaping modulation. These inputs provide real-time current measurement, fault protection (e.g., over-current), and control calibration to mitigate external component errors (e.g., shunt resistor tolerances).

The Σ-Δ architecture achieves higher resolution by extending the sampling duration of the 1-bit output bitstream, while parallel analog comparators enable sub-100 ns over-current protection (OCP) independent of the ADC's digital processing latency. Calibration registers adjust offset and gain to align sensed values with system requirements, ensuring robust operation across load transients and temperature variations.

Input Current Sense

Current Sense 1 (CS1) is typically used for the monitoring and protection of the primary side current, which is commonly sensed using a current transformer (CT). The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.6 V. The input signal is also fed into an analog comparator for cycle-by-cycle current limiting and IIN over-current fast protection, with a reference of 0.25 V or 1.2 V. The typical configuration for the CS1 current sense is shown in Figure 3.

Input current information with default scale in the READ_IIN command (Register 0x89), with an asynchronously averaged rate of 0.655 ms. IIN_CAL_GAIN stores the scale ratio of CT turns ratio and sense resistance, which used to generate READ_IIN. Various IIN over-current fast fault limits and response actions can be set for CS1.

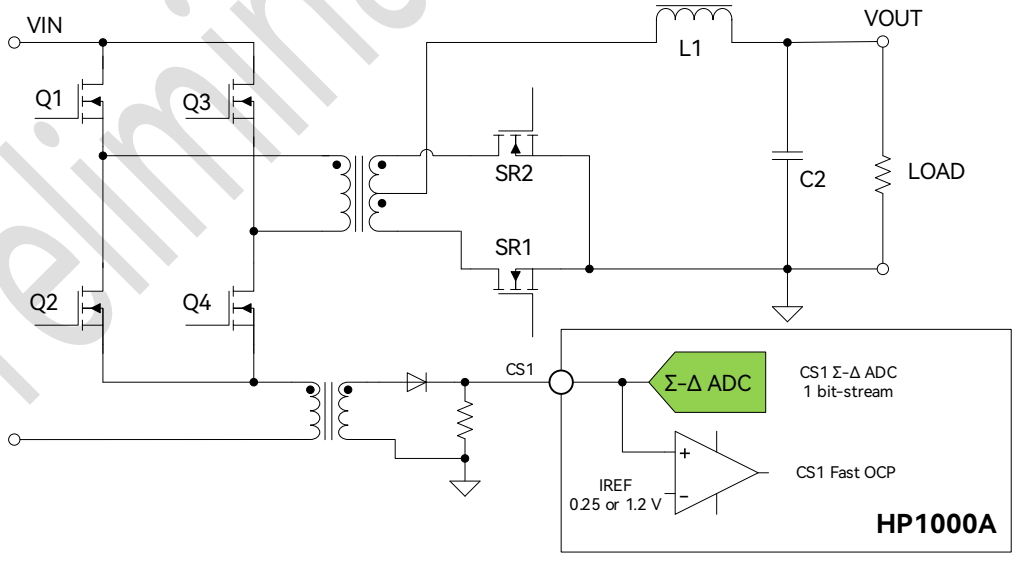


Figure 3 Diagram of CS1 Primary Current Sense

Output Current Sense

The CS2+ and CS2− pins are differential inputs used for the monitoring and protection of the secondary side current. The HP1000A supports differential sensing using low-side current sensing with two ranges for the ADC: 30 mV and 60 mV, as shown in Figure 4.

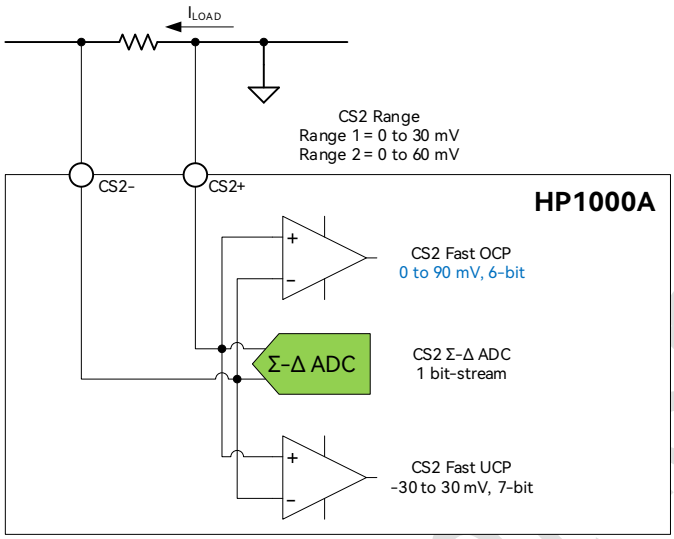


Figure 4 Diagram of CS2 Low-Side Resistive Current Sense

An additional range of 240 mV (single-ended input only) can be used for high-side sensing or simply as an input with a higher range, as shown in Figure 5. The high input range is used for operation in single-ended mode, where external circuitry must be provided for the current signal.

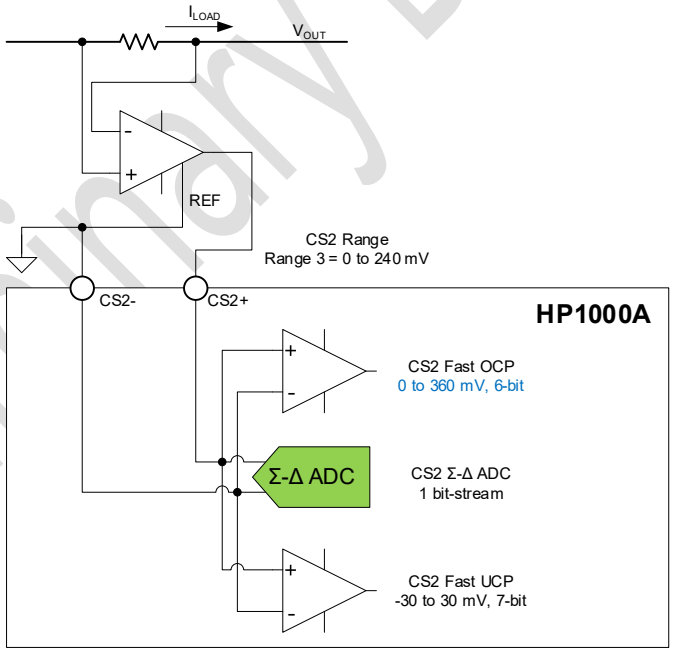


Figure 5 Diagram of CS2 High-Side Resistive Current Sense

The HP1000A reports output current readings via the READ_IOUT command (Register 0x8C), with an asynchronously averaged rate of 0.655 ms. IOUT_CAL_GAIN (0x38) and IOUT_CAL_OFFSET (0x39) are used to calibrate the READ_IOUT value. The 12 MSBs of the reading are converted into PMBus format and compared against configured thresholds for fault decisions. Thresholds and limits for CS2 can be configured using PMBus commands:

- IOUT_OC_FAULT_LIMIT (Register 0x46)
- IOUT_OC_WARN_LIMIT (Register 0x4A)

It should be noticed that the CS2 maximum over-current protection threshold can be set to 90 mV (using 30 mV or 60 mV ADC range setting) and 360 mV (using 240 mV ADC range setting).

CONTROL LOOP

Digital Compensator

Use the internal programmable digital compensator to change the control loop of the power supply. Feedback voltage from VS± pins and converted by tracking ADC. The data updating rate of tracking ADC is 25 MHz. Voltage loop compensator will calculate at least once in one switching period, therefore, before PID compensator updates the duty cycle, feed-back voltage will be averaged from previous switching period until next calculation.

A Type III digital compensator architecture has been implemented considering one switching cycle delay due to the duty cycle update method. From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$G(z) = \frac{k_I}{1 - z^{-1}} + \left(k_P + k_D \frac{1 - z_0 z^{-1}}{1 - p_1 z^{-1}}\right) \frac{1 - p_2}{1 - p_2 z^{-1}}$$

where,

k_P, proportional gain.

k_I, integral gain.

k_D, derivative gain.

z_0, zero of derivative part.

p_1, pole of derivative part.

p_2, additional high frequency pole, can be disabled.

Double Update Rate

The HP1000A updates the duty cycle once per period based on a sample taken just before the period starts. Because a transient can happen at any time, this method creates a phase delay equal to $D \times t_{SW}$, as the new command must wait nearly a full cycle to take effect.

The control loop exhibits an inherent latency of $D \times t_{SW}$, as the duty cycle command requires this period to take effect. This phase delay, which becomes more pronounced near the switching frequency, can limit the achievable crossover frequency and degrade the phase margin. The HP1000A mitigates this issue by employing a duty-cycle double-update-rate scheme. Specifically, it samples the output voltage shortly before the mid-point of the switching half-cycle and updates the duty command accordingly. This technique effectively reduces the phase delay to $D \times t_{SW} / 2$.

Fast Input Voltage Feed-Forward

The HP1000A supports voltage line feed-forward control to enhance line transient performance. When the VFF input is 1 V, the line feed-forward remains neutral. For instance, if the digital filter output remains constant while the VFF voltage drops to 50% of its nominal value (while maintaining a minimum of 0.5 V), the modulation of the main switches' falling edges doubles. This voltage line feed-forward function is configurable via Register FFWD_SETTING and is recommended to be enabled during soft start.

The VFF pin voltage must be calibrated to 1 V under nominal input voltage conditions. The VFF voltage is sampled in 25 MHz, enabling real-time PWM output adjustments based on input voltage changes. The feed-forward mechanism typically detects input voltage transients over 3.125% of the average VFF value in previous switching period and responds by modifying PWM outputs within a single switching cycle; otherwise, the averaged VFF value in current switching period will be used for feed-forward calculation.

An integrated ADC connected to the VFF pin provides input voltage telemetry. The primary input voltage can be derived using the formula:

$$V_{\mathrm{PRI}} = V_{\mathrm{RECT}} \times \frac{R_{\mathrm{FU}} + R_{\mathrm{FD}}}{R_{\mathrm{FD}}} \times n$$

where V_{RECT} is the measured voltage at the VFF pin, n is transformer turns ratio.

For fault management, the input voltage monitored by the VFF ADC is converted to PMBus format using the 11 MSBs of the reading. Fault thresholds and responses are programmable through PMBus commands, including

VIN_UV_FAULT_LIMIT (0x59), VIN_OV_FAULT_LIMIT (0x55), VIN_UV_FAULT_RESPONSE (0x5A), and VIN_OV_FAULT_RESPONSE (0x56).

PWM

PWM Outputs

The PWM outputs are used to control the primary-side drivers and synchronous rectifier drivers. They support multiple topologies, including hard-switched full-bridge, half-bridge, push-pull, two-switch forward, active clamp forward, multi-phase buck, switch-cap buck, and others. The delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoot-through and cross-conduction.

It is recommended to use the HP1000A GUI software to configure these outputs. Figure 6 illustrates an example configuration for driving a hard-switching full-bridge topology with synchronous rectification, as shown in Figure 33. The Q1, Q2, SR1, and SR2 switches are individually driven by the PWM outputs. Both the rising and falling edges of each PWM signal can be independently programmed, and either edge can be configured as a modulated edge that adjusts dynamically based on the modulation result per PWM period.

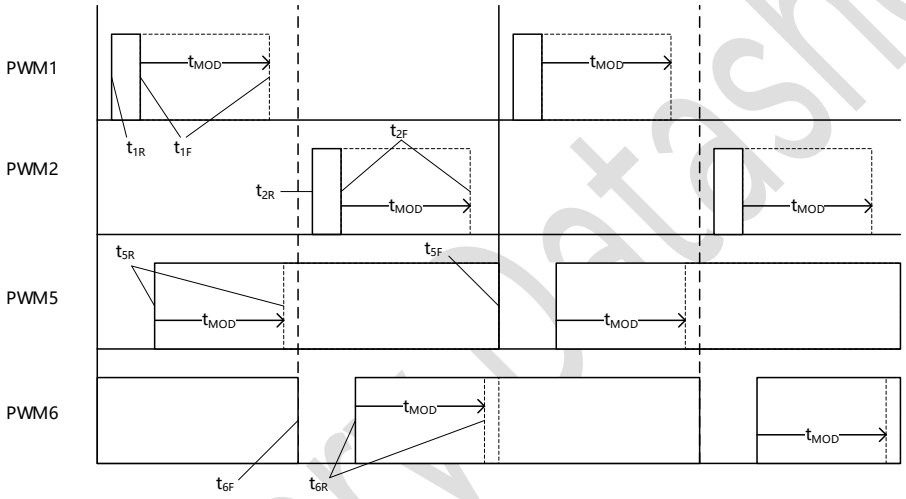


Figure 6 PWM Configuration for Full-bridge Converter

The PWM1 to PWM6 outputs are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all of the registers and then latch the information into the shadow registers at one time. During the reprogramming operation, the outputs are temporarily disabled. To ensure that new PWM timings and the switching frequency setting are programmed simultaneously, a special instruction is sent to the HP1000A by setting the Confirm commands. It is recommended that the PWM outputs not in use be disabled.

Frequency Synchronization

The HP1000A features a frequency synchronization function that includes a synchronization input for operating as a slave device (SYNC_IN) and a synchronization output for functioning as a master device (SYNC_OUT). Both functions can be configured using the SYNC pin (Pin 22).

Synchronization as a Slave Device

The HP1000A features a SYNC pin for frequency synchronization. The internal digital phase-locked loop (DPLL) detects the master frequency on the SYNC pin (f_{SYNC}) and locks the internal switching frequency to the external source. The maximum lock/capture range is ±12.5% of the programmed switching frequency (set via FREQUENCY_SWITCH command, Register 0x33).

PWM outputs synchronize to the PWM1 pin at the start of each switching period. For example, if PWM1's rising (or falling) edge occurs at x µs after the switching period begins (t = 0), synchronization aligns the time difference between the external master synchronization signal's rising edge (f_{SYNC}) and PWM1's edge to maintain x µs. All other PWM outputs adjust proportionally, ensuring phase coherence during synchronization.

The INTERLEAVE command (Register 0x37) enables phase shifts in as 360°/(group number) increments. This command also configures group IDs and device numbering within groups.

The HP1000A supports discrete switching frequencies due to its 5 ns PWM resolution. Note that the switching frequency and master clock frequency may not be exact multiples of each other. If the master clock abruptly stops (0

Hz), the HP1000A continues operating at the last synchronized frequency, as presented in Figure 7. During a soft-start power cycle, the device reverts to the internal frequency defined by FREQUENCY_SWITCH (Register 0x33). If powered on while a master frequency is present on the SYNC pin, the HP1000A immediately locks to the external frequency.

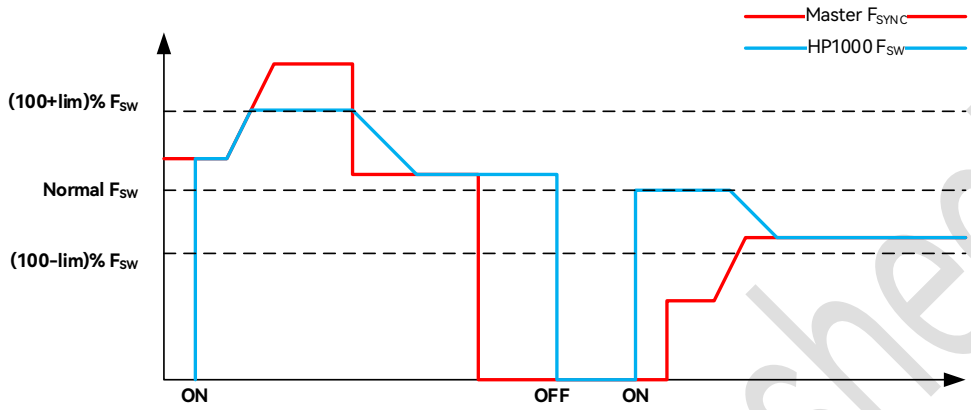


Figure 7 Synchronization Operation. Stay in Last Synchronized Frequency when Lost Synchronization

The HP1000A also supports fold-back to normal frequency defined in 0x33 command as depicted in Figure 8.

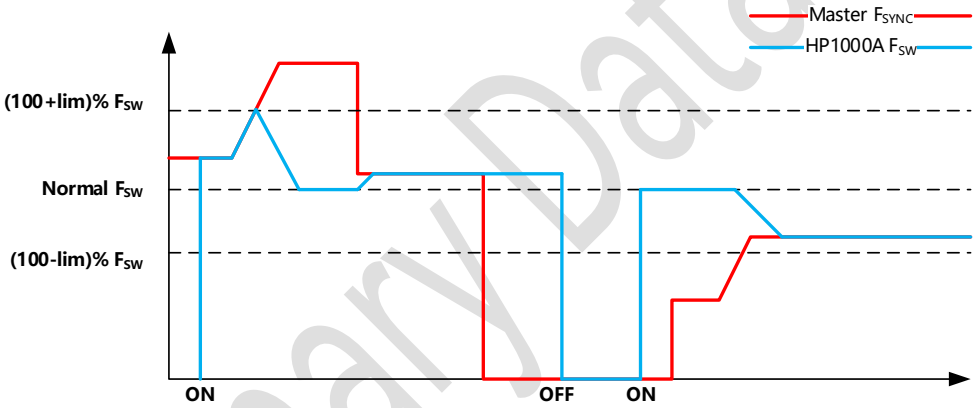


Figure 8 Synchronization Operation. Fold-back to Normal Synchronized Frequency when Lost Synchronization

Disable synchronization when unused to prevent switching noise coupling into the SYNC pin.

Synchronization as a Master Device

The SYNC pin of the HP1000A can be configured for synchronization output (SYNC_OUT) functionality, allowing the SYNC pin (Pin 22) to generate a synchronization reference clock output. When synchronization master mode is enabled, SYNC produces a 640ns-pulse-width clock signal corresponding to the internal switching frequency.

To compensate for propagation delays in the HP1000A synchronization scheme, the synchronization output signal maintains a 760 ns lead time prior to the internal switching cycle initiation.

The synchronization output remains active when VDD is powered, except for VDD_OV fault conditions which immediately disable the synchronization output.

HiZ Mode

The PWM1 and PWM2 channels support open-drain output mode for driving DrMOS which requires tri-state PWM inputs, by setting their respective configuration bits. During power-up and in disabled states, the PWMx outputs are both high-impedance to prevent unintended current flow. If a PWMx channel is configured in open-drain output mode, the output will remain high-impedance under the following conditions: When the HP1000A enters idle state, or upon detection of fault states.

Digital PWM Dithering

The PWM dithering is done by making the PWM duty-cycle not constant any more. The idea is to adjust the duty-cycle by one LSB with a repetitive pattern over a given number of consecutive PWM periods. An external low-pass filter is

used to cut the extra switching components and the result consists in an added DC offset with a resolution less than one duty cycle LSB. The duty-cycle adjustment can be made following two possible approaches.

- The first approach consists in subtracting one LSB from the periods where a duty-cycle adjustment should be made. In this case the DC offset is going to be negative.
- The other way is by adding one LSB to the periods where a duty-cycle adjustment should be made. In this case the DC offset is going to be positive.

The added DC offset is proportional to the ratio between the number of PWM periods where duty-cycle adjustment is made, divided by the number of consecutive PWM periods making one PWM dithering pattern. Whatever the duty-cycle adjustment pattern, the obtained ratio is always a positive sub-one fractional value. With this dithering technique, external devices can be controlled with a higher resolution than the original PWM resolution.

Figure 9 Consists of PWM Pulse Width

HP1000A supports 4-bit digital PWM dithering, the dithering-added resolution bits controls a look-up table to add one-LSB to duty cycle output.

Active Snubber Control

The active clamp signals turn on after a selectable dead time (0 ns to 315 ns in steps of 5 ns). The signals can be configured on one of the following:

- Falling edge of PWM5 or PWM6 signal
- Rising edge of PWM3 or PWM4

The snubber signal stays on for a fixed value regardless of the duty cycle and load condition programmed in Register GPIO3_4_SNUBBER_ON_TIME. However, the snubber signal is toggled as soon as it encounters the next PWM5/6 rising edge or the next PWM3/4 falling edge, even if the programmed-on time is of a greater value.

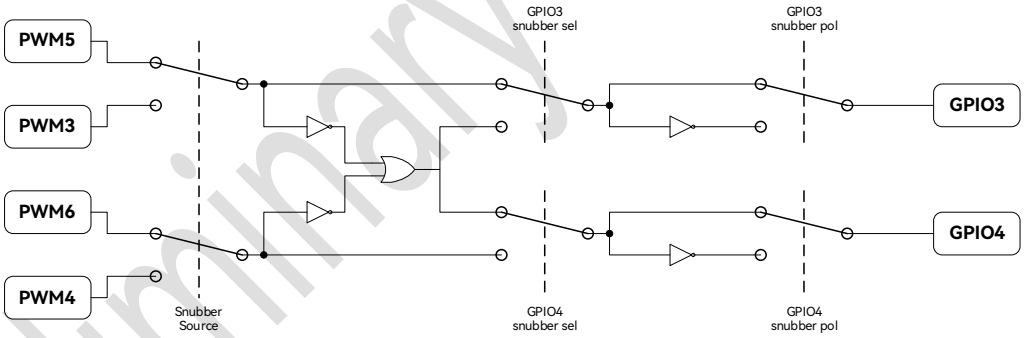


Figure 10 GPIO3 and GPIO4 Snubber Configuration

It should be notice that when PWM3 or PWM4 is configured as active snubber control, the PWM3/4 signals output from the PWM generator are used as internal signals for the snubber control logic.

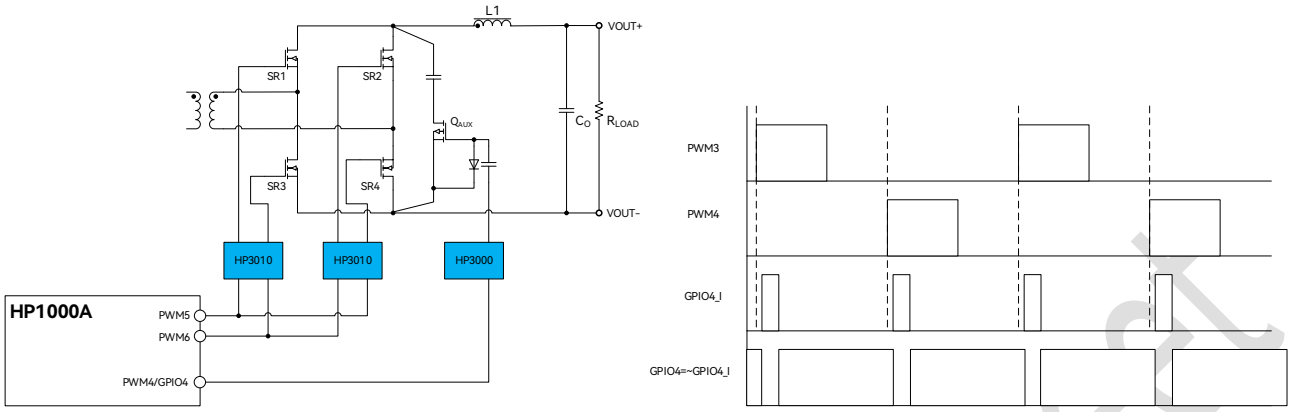


Figure 11 Active Snubber for Full-bridge Converter and Timing of Control Logic

Figure 11 illustrates an example of applying an active snubber to the SR (synchronous rectifier) in a hard-switching full-bridge converter, along with its control timing diagram.

Open-drain Output Mode

PWM1 to PWM6 support open-drain output mode for driving DrMOS by setting corresponding bit, which requires a tri-state PWM input. The powering-up and disabled state of PWMx are high-impedance. If PWMx is configured as open-drain output mode, PWMx will be high-impedance if the device is in idle or fault state.

NORMAL OPERATION

ON/OFF Control

The OPERATION command (Register 0x01) and ON_OFF_CONFIG command (Register 0x02) collectively govern the power management functionality of the HP1000A. The OPERATION command controls the HP1000A's power state in conjunction with the CTRL pin (Pin 23), while the ON_OFF_CONFIG command determines the specific logic combination required for power state transitions between CTRL pin inputs and PMBus commands.

When activating the HP1000A through valid control signals, the Power Supply On (PSON) signal initiates a controlled soft-start sequence. This procedure systematically ramps up the power conversion process, ensuring stable operation during startup. Conversely, shutdown commands trigger a coordinated power-down sequence that follows configured fault response protocols. Both operational states maintain strict adherence to the configured parameters in the ON_OFF_CONFIG register for state transition validation.

Soft Start

Following VDD power stabilization and system initialization, the HP1000A activates the PSON signal upon receiving a valid turn-on command. A user-configurable delay period (TON_DELAY) precedes the soft-start sequence, ensuring system stability before voltage ramp initiation, as presented in Figure 12. During soft start, the controller employs closed-loop regulation to gradually elevate the output voltage to the programmed setpoint. The TON_RISE parameter precisely defines the ramp duration (0 to 100 ms, 1 ms resolution), mitigating inrush currents through controlled voltage slew rate adjustment. Pre-biased output conditions trigger adaptive timing logic, dynamically compressing the rise phase while extending the initial delay to accommodate existing voltage levels.

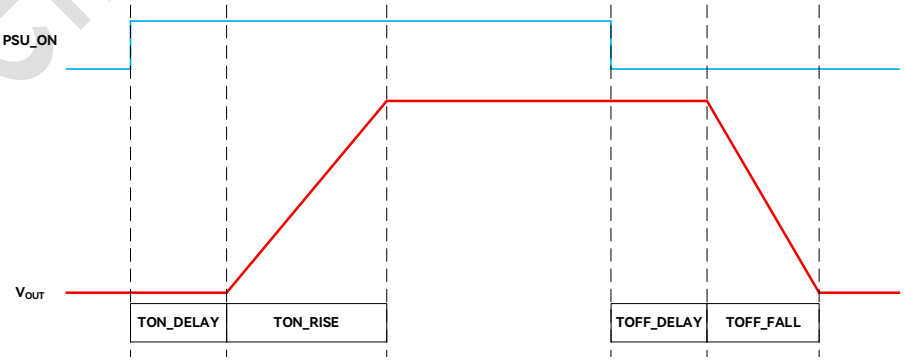


Figure 12 Soft-start and Soft-stop Settings

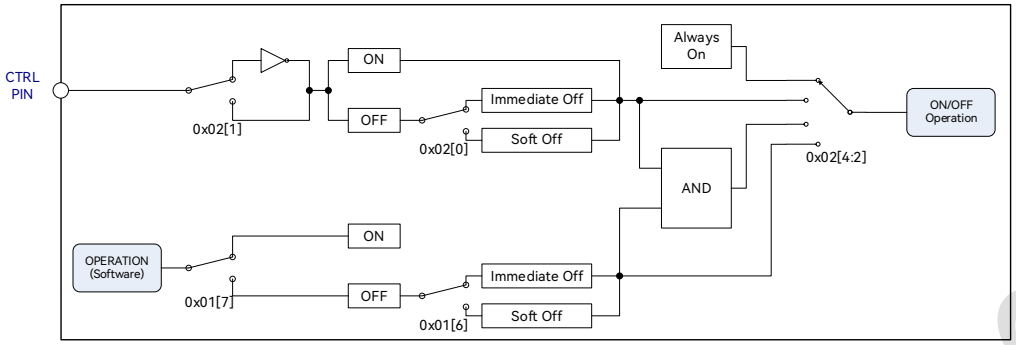


Figure 13 On/Off Control Diagram

Power state transitions are controlled by registers, providing granular control over operational timing,

- Turn-On Delay (TON_DELAY):0 to 1023 ms delay post-command execution (1 ms resolution)
- Turn-Off Delay (TOFF_DELAY):0 to 1023 ms delay before shutdown initiation (1 ms resolution)
- Voltage Ramp-Down (TOFF_FALL): 0 to 100 ms output discharge duration (1 ms resolution)

These parameters enable precise synchronization with downstream power stages and system-level sequencing requirements. All timing values are rounded to the nearest integer multiple of their respective resolution steps. Out-of-bound programming attempts automatically clamp to valid extremes:

- Values exceeding maximum ranges adopt ceiling limits
- Sub-minimum entries default to floor values
- This fail-safe mechanism ensures operational integrity across all configuration scenarios.

Figure 13 On/Off Control Diagram illustrates the hierarchical interaction between command signals, delay phases, and voltage ramp profiles.

Soft Stop

The soft stop process mirrors the soft start mechanism, utilizing the TOFF_DELAY, TOFF_MAX, and TOFF_FALL commands, which correspond to the TON_DELAY, TON_MAX, and TON_RISE parameters used during startup. The HP1000A implements soft stop functionality through two operational modes:

- Controlled shutdown: Activated via the OPERATION and ON_OFF_CONFIG commands for normal power supply termination.
- Fault-triggered shutdown.

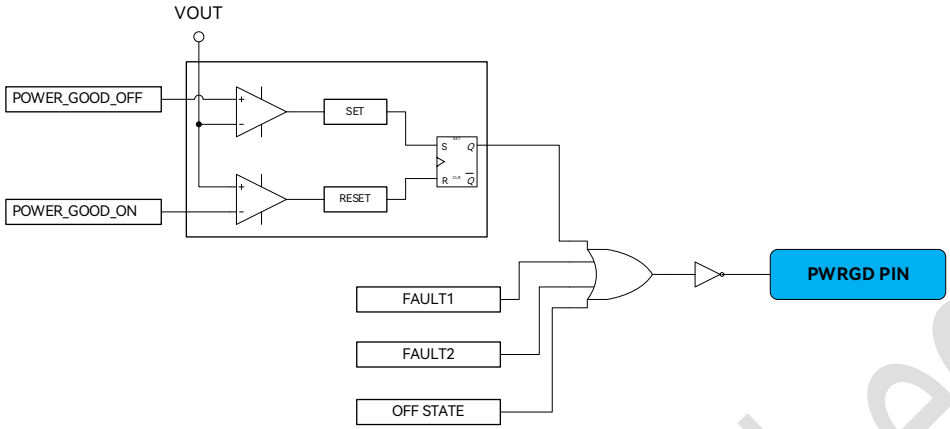
Soft stop timing is defined by the TOFF_DELAY (Register 0x64) and TOFF_FALL (Register 0x65) parameters. During this process, critical faults (e.g., OTP, OVP, GPIO) can be masked via corresponding configurations. To ensure complete discharge, the SR1 and SR2 PWM outputs remain active for an extended period.

PWRGD Signals

The POWER_GOOD_ON register (Register 0x5E) defines the minimum output voltage threshold required to assert the POWER_GOOD signal. Conversely, the POWER_GOOD_OFF threshold (Register 0x5F) specifies the voltage level below which POWER_GOOD is deserted. Its status is also readable through the STATUS_WORD register (0x79[11]). PWRGD asserts (logic 0 means power is good) only when all following criteria are satisfied:

- VOUT has exceeded POWER_GOOD_ON.
- VOUT has not fallen below POWER_GOOD_OFF.
- FAULT1 is not set.
- FAULT2 is not set.

UVP is not associated with this flag; however, the FAULT1 and FAULT2 flags can be programmed to select UVP (VOUT_UV_FAULT). There is no debounce for PWRGD output.



VOUT		Q
< POWER_GOOD_OFF	SET=1	1
> POWER_GOOD_ON	RESET=1	0

Q	OFF STATE	FAULT1	FAULT2	POWER_GOOD
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Figure 14 Diagram of PWRGD Signal

OPEN-LOOP OPERATION

The HP1000A can also run in open-loop operation mode. In this mode, the rising edges and falling edges of the PWM outputs are fixed during normal operation. Therefore, the output voltage varies with the input voltage. The topologies include full bridge, half bridge, and push pull converters.

The PWM settings of open-loop operation are different from those of general closed-loop operation. Set the rising edge timings and falling edge timings by using Register 0xFE01 to Register 0xFE0C. Typically, a duty cycle setting of ~50% is recommended for ease of zero-voltage-switching operation. A phase shift function of 180° is preferred to guarantee balanced PWM outputs. Those PWM outputs are not enabled for open-loop operations will follow the closed-loop operation rules.

Apply negative modulation to the falling edges of all PWM outputs, PWM1 to PWM4 (or just one pair of them), for soft start. If modulation enabled for PWM1 to PWM4 or PWM5/PWM6, soft start will be applied for these PWM outputs. The soft start of PWM5 and PWM6 is not recommended.

PWM channels which are not selected for open-loop operation will operate as normal mode. Because the output voltage is not regulated, some of the settings, such as the V_{OUT} setting, digital compensator settings, and constant current control, are not functional. Other settings can be programmed to be like those of general closed-loop operation.

Open-Loop Soft-Start

To achieve a more linear and smoother output voltage during open-loop soft-start, the implementation of multi-segments soft-start of duty and switching frequency is recommended. This approach ensures smoother voltage ramps, enhancing system performance and reducing potential stress on components.

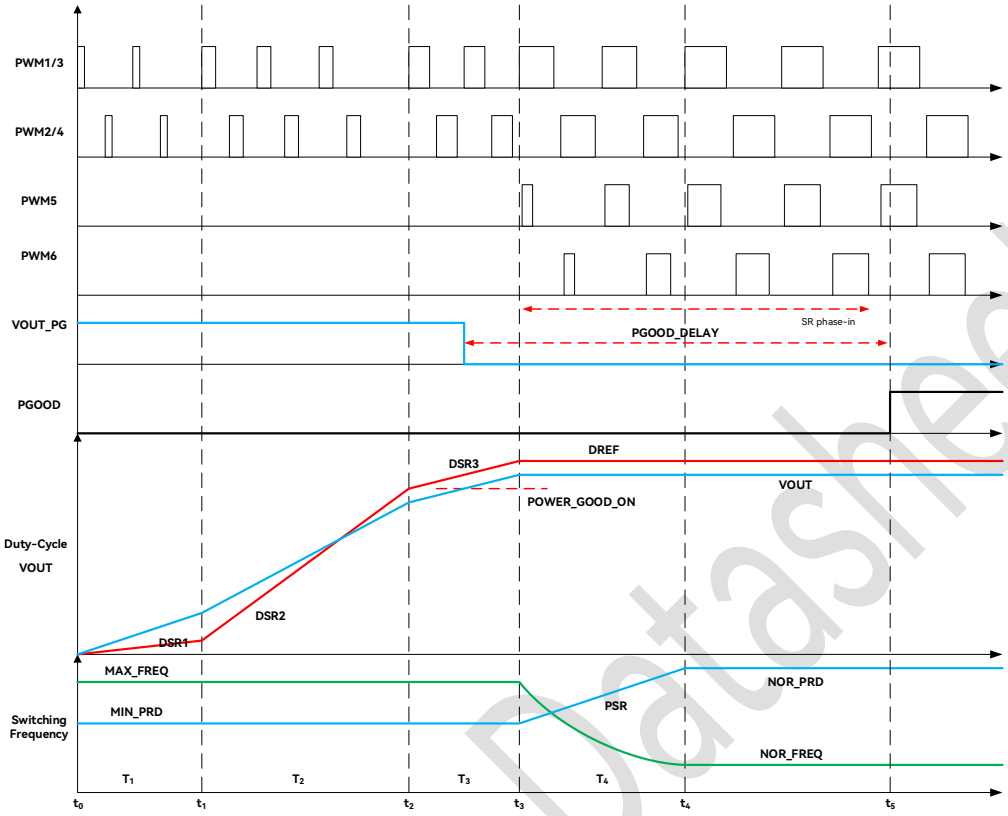


Figure 15 Diagram of Multi-segments Soft-start Timing

PWM Configuration for Open-Loop LLC and Dead-Time Scheme

When T4 ≤ 0, PWM and dead-time configurations are the same as closed-loop, which is generated by the edge arrangement. For open-loop LLC applications (T4 > 0), it should be noticed that the switching period increases, and the duty cycle is clamped at nearly 50%. The dead-time between primary switches should not be changed as shown in Figure 16.

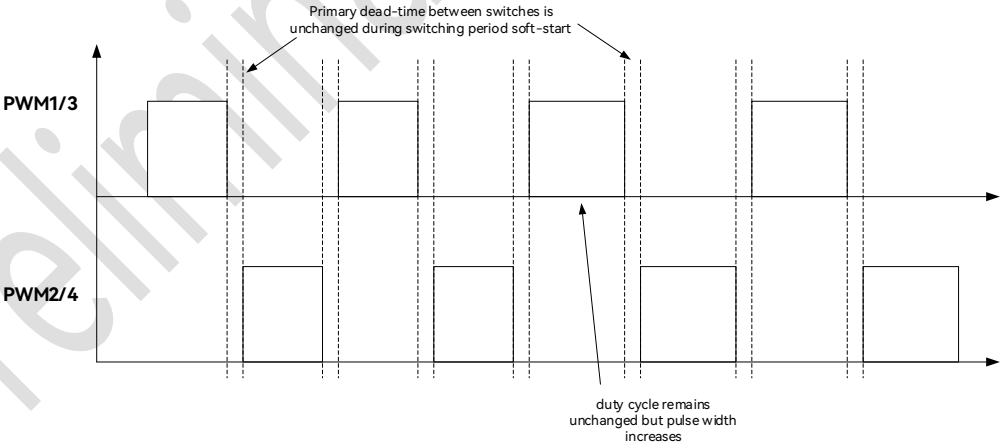


Figure 16 Primary Dead-time between Primary Switches during Switching Period Soft-start

Turn-on and turn-off delays are introduced to the secondary regulator (SR), specifically for PWM5 and PWM6, in open-loop LLC applications, as described in the documentation. The SR will turn on with a delay of t_{on_dly} after the primary-side PWM pulse turns on. Additionally, the SR will turn off with a delay of t_{off_dly} before the primary switch turns off.

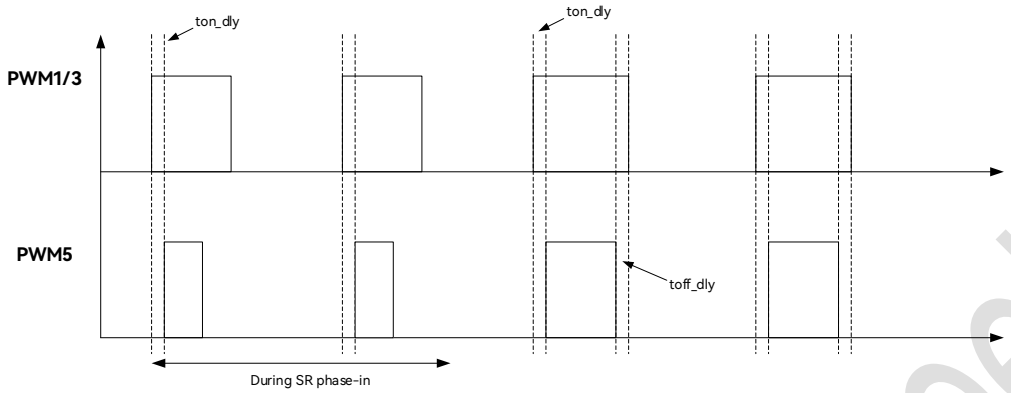


Figure 17 SR Dead-time during SR Slow-Ramping and Normal Operation

SR Slow-Ramping During Soft-start

Figure 17 illustrates the SR slow-ramping during soft-start. SR slow-ramping initiates after T3 and follows a closed-loop configuration, including slow-ramping enables control, slow-ramping speed adjustment, and fast ramping capability. Note that for open-loop LLC applications (where T4 > 0), the SR pulse width at the end of slow-ramping equals the current primary pulse width minus (t_{on_dly} + t_{off_dly}).

SR Slow-Ramping During Soft-Stop

If T4 ≤ 0, SR slow-ramping during soft-stop follows closed-loop configuration. It should be noticed that, for open-loop LLC applications (T4 > 0), soft-stop is not supported. And SR slow-ramping during soft-stop will be discard, PWM5 and PWM6 will be turned-off immediately when power supply is switched to off-state.

PRE-BIAS START

The pre-bias start-up function provides the capability to start up with a pre-biased voltage on the output. It protects the power supply against existing external voltage on the output during startup and ensures a monotonic startup before the power supply reaches full regulation (see Figure 18).

During pre-bias startup, the HP1000A soft start ramp starts at the existing voltage value sensed on the VS± pins, and the soft start ramp time is reduced proportionally. The initial PWM modulation value does not begin with zero but, instead, with a value that builds a balanced relationship between the input voltage and the output voltage. This balance avoids the sudden charging or discharging of the output capacitor and achieves a monotonic and smooth startup. The initial modulation value is calculated by the following equation:

$$D_{PRE} = D_{REF} \times \frac{V_{OUT}}{V_{REF}} \times \frac{V_{IN\_NOR}}{V_{IN}}$$

where:

- D_{PRE} is the initial duty-cycle when the controller begins to generate PWM pulses during startup.
- D_{REF} is the reference duty-cycle set by Register OPL_DREF (re-use open-loop reference duty). It emulates the duty cycle when the input voltage and the output voltage are in nominal condition.
- V_{OUT} is the sensed output voltage.
- V_{REF} is the nominal output voltage set by VOUT_COMMAND (Register 0x21) and scaled based on VS ADC resolution.
- V_{IN_NOM} is the nominal input voltage when the VFF pin voltage = 1 V.
- V_{IN} is the sensed input voltage.

If pre-bias duty is enabled, a pre-set duty cycle will be loaded to PID compensator for generating an initial duty cycle. The initial modulation value is calculated as,

$$i\_term\_init = \frac{V_{OUT}}{V_{REF}} \times D_{REF}$$

where:

- *i_term_init* is the initial duty cycle of PID compensator when the controller begins to generate PWM pulses during startup. It should be noticed that the i_term_init will be loaded to PID compensator only once before soft start.

- D_{REF} is the reference duty-cycle set by Register OPL_DREF (re-use open-loop reference duty). It emulates the duty cycle when the input voltage and the output voltage are in nominal condition.
- V_{OUT} is the sensed output voltage.
- V_{REF} is the nominal output voltage set by VOUT_COMMAND (Register 0x21) and scaled based on VS ADC resolution.

It should be noticed that it should consider setting current VS value as initial ramp-up reference voltage, especially that VS > VOUT_COMMAND. And the slew-rate of reference ramp should be the same as the one set by TON_RISE and VOUT_COMMAND.

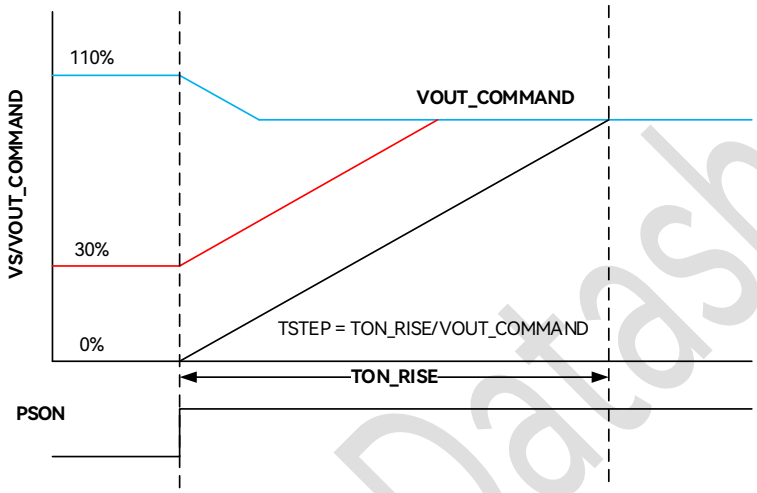


Figure 18 Pre-bias Start and VOUT_COMMAND

If the closed-loop line voltage feed-forward function is selected, the input voltage is introduced from the feed-forward loop, and the V_{IN} value is always included for calculation of the initial modulation value. SR reverse current protection can be used in pre-bias start-up mode. SR soft start can also be enabled in this mode to achieve a smooth transition.

Primary Voltage Sense before Start-up

In isolated power topologies, primary-side voltage sensing can be implemented using an auxiliary winding from the power supply. For such applications, the VSET pin must be configured to primary voltage sense mode. Note that this mode is mutually exclusive with the DOSA trim function.

Additional Pre-bias Duty

Additional pre-bias duty is provided for adjusting V_{OUT} pre-bias performance, eliminating voltage drop when calculated duty is less than desired value. A 2-bit option is provided, 1.5625%/LSB, and ranges from 0 to 4.6875%.

Non-linear Mode for Switch-cap Converter

The HP1000A supports non-linear pre-bias duty mode. The voltage-conversion ratio *M* of switch-cap application on duty cycle is non-linear, as following described,

$$M = \frac{V_{OUT}}{V_{IN}} = \begin{cases} \frac{D}{2} & d < 0.5 \\ D^2 & d > 0.5 \end{cases}$$

And,

$$D = \begin{cases} \frac{2V_{OUT}}{V_{IN}} & d < 0.5 \\ \sqrt{\frac{2V_{OUT}}{V_{IN}} \times \frac{1}{2}} & d > 0.5 \end{cases} \quad (1)$$

Therefore, it supports non-linear pre-bias start-up duty calculation for switch-cap applications. The pre-bias duty can be expressed as Equation 1, and the reference duty cycle D_{REF} can be set through register.

$$D_{REF} = \frac{2V_{REF}}{V_{IN\_NOR}}$$

GPIO FUNCTIONS

PWRGD, SYNC, PWM3, PWM4, and PWM6 feature multiple programmable functions. The following Table 5 lists all alternate functions of these configurable GPIO pins.

Table 5 GPIO1 to GPIO4 and GPIO6 Pin-mux Configurations

Functions	GPIO1	GPIO2	GPIO3	GPIO4	GPIO6
1	PWRGD Output	SYNC	PWM3	PWM4	PWM6
2	External Fault 1 Input	External Fault 2 Input	Snubber PWM A	Snubber PWM B	R_{ISHARE} control
3	FAULT1 Output	FAULT2 Output	External Fault 3	External Fault 4	/
4	/	PWRGD Output	R_{ISHARE} control	/	/

GPIO1 to GPIO4 can be set as external fault input. The fault response will be set by GPIO1_FAULT_RESPONSE and GPIO2_FAULT_RESPONSE and GPIO3_4_FAULT_RESPONSE (GPIO3 and GPIO4 shared one response). The fault debounce time is set by DEBOUNCE_SETTING_4.

CONSTANT CURRENT MODE

The HP1000A integrates an advanced constant-current output function with fast dynamic response. This mode can be disabled via configuration settings.

The built-in Σ-Δ ADC on CS2+/CS2- pins performs conversion on the sampled output current. The results, which are used for constant-current loop calculation, support three programmable precision configurations: 6-bit/2.56 μs, 7-bit/5.12 μs, and 8-bit/10.24 μs. This allows users to optimize the trade-off between current-sharing response speed and accuracy according to system requirements. The constant-current target threshold is set by the IOUT_OCP_FAULT_LIMIT register. The error between this set value and the real-time sampled output current is fed into a PI compensator. The loop calculation generates a constant-current control signal, which achieves precise regulation by adjusting the output voltage.

OUTPUT VOLTAGE DROOP (VDROOP) CONTROL

The VDROOP sharing functionality is implemented using the VOUT_DROOP command (Register 0x28). Using this command, a fixed amount of load line in mV/A can be applied to the output voltage. The output voltage is continuously sampled with a selectable rate before the droop is applied. Under VDROOP current sharing, the output voltage changes at a rate determined by the VOUT_TRANSITION_ RATE command. The internal voltage reference can be set to the fastest internal supported rate.

ACTIVE CURRENT SHARING

The IMON pin provides a current-source DAC output reflecting the output current, serving dual purposes for both current monitoring and active current balancing in multi-module parallel configurations. This pin sources a configurable current proportional to the output current via a 6-bit DAC with 4-bit dithering enhancement, achieving effective 10-bit resolution over a 0 to 640 μA range. The DAC's full-scale current (640 μA) corresponds to maximum load, whereas 320 μA represents no-load conditions, with values below 320 μA indicating negative current flow.

A precision 2.49 kΩ ±0.1% resistor (R_{ishare}) between IMON and ground converts the current signal to voltage (1.6 V at full load, 0.8 V at no-load). A parallel 1 nF capacitor is recommended to mitigate dither-induced ripple. In parallel systems, interconnected IMON pins establish a shared voltage representing average current, enabling individual modules to self-correct against this reference.

Current sharing incorporates a dead zone to prevent oscillation during minor current deviations. Voltage clamping protects output regulation during significant current imbalances, triggering fault reporting when reaching voltage limits while current errors exceed the dead zone threshold.

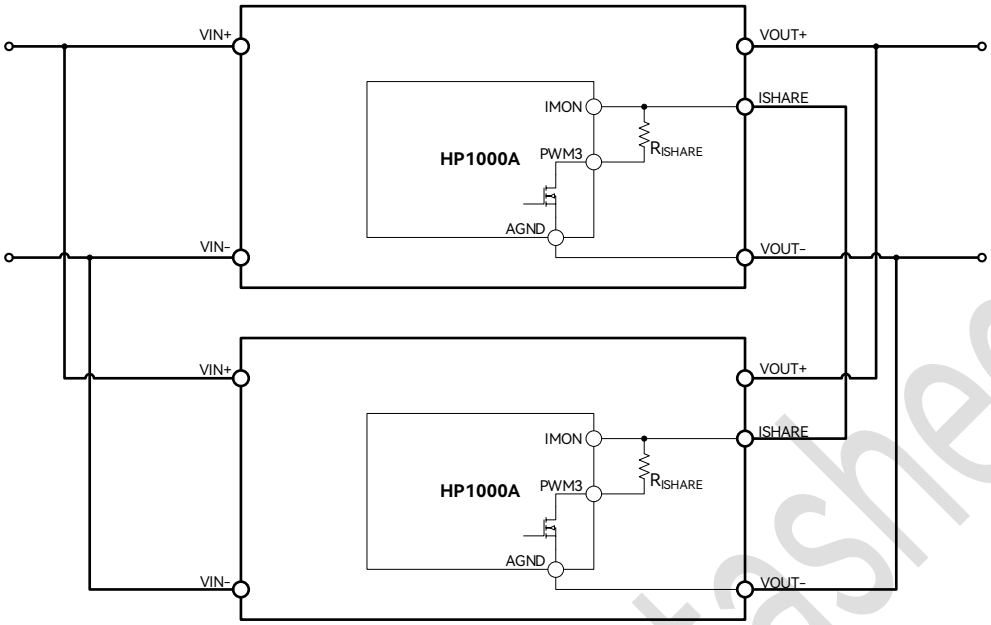


Figure 19 parallel module current sharing.

Current Sharing Resistor Control

The R_{ISHARE} resistor is connected between the IMON pin and the output ground. This configuration yields inaccurate average current data if one or more parallel units are inactive, for instance, during turn-on delay or protective shutdown. When the unit is disabled, the R_{ISHARE} resistor remains in parallel with others on the IMON bus, reducing the total equivalent resistance and causing the HP1000A to report a lower-than-actual average current.

Therefore, the R_{ISHARE} resistor should be disconnected from the IMON bus when the converter is not operating. PWM3 and PWM6 pins feature open-drain output mode. These outputs default to a high-impedance (Hi-Z) state when the HP1000A is unbiased, permitting connection to an external voltage before VDD is applied. Consequently, PWM3 and PWM6 can function as switches to float the R_{ISHARE} resistor when the device is disabled and connect it to ground when enabled.

TEMPERATURE SENSE

DrMOS Mode and Fault Detection

The TSNS/FLT pin on HP1000A supports DrMOS temperature sensing with a linear voltage output proportional to junction temperature. The output follows a characteristic of 8 mV/° C with a 0.6 V offset at 0° C, expressed as,

$$V_{TOUT} = 8mV \times T_J + 0.6V$$

For integration, the input voltage is scaled to half before ADC sensing to accommodate the range, as the voltage at T_J = 150 ° C reaches 1.8 V, exceeding typical ADC limits. The sensing spans a theoretical temperature range of -75 ° C to 150 ° C, correlating to 0 V to 0.9 V. This is converted to a digital code via internal built formula and user trim settings can adjust the temperature reading result.

The TSNS/FLT pin also enables fault detection for DrMOS, indicating catastrophic events like over-temperature, phase fault, and over-current by pulling up to 3.3 V. In multi-phase configurations, tying these pins together allows the highest temperature or fault to drive the bus. Internally, HP1000A integrates a programmable 4-bit DAC with a range of 0.625 V to 2.5 V and a comparator for fault detection, supporting configurable output polarity to accommodate different fault signaling types.

NTC Mode

The HP1000A linearization scheme for NTC mode is designed for optimal performance when linearizing temperatures within the industrial range. It utilizes a specific combination of components: an NTC thermistor with R_{25} = 100 kΩ (1%), a 16.5 kΩ (1%) external resistor, and the integrated 46 μA current source.

The required NTC thermistor, such as the NCP15WF104F03RC, must have a resistance of R_{25} = 100 kΩ at 1% tolerance. For best accuracy, we recommend using 1% tolerance components for both the external resistor and the

thermistor's beta value. The linearization equations show the relationship between the NTC voltage, V_{NTC} (in volts), and temperature reading, *T* (in degrees Celsius). *T* represents the temperature reading in Register 0x8D.

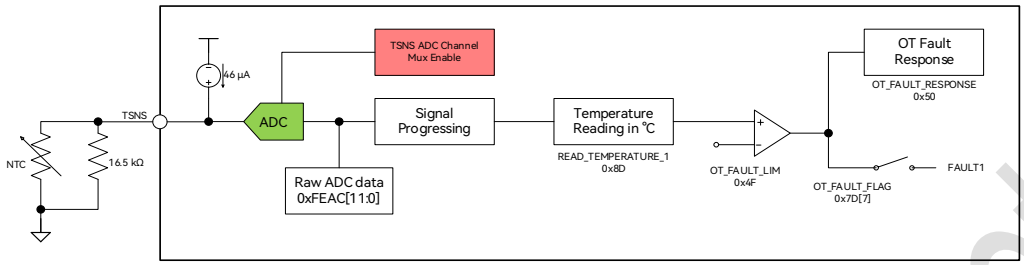


Figure 20 TSNS and OTP Operation

ADDRESS DETECTION

The HP1000A operates through an I²C interface, functioning as a PMBus-compliant slave device on the bus. Its programmable PMBus slave address is configured via an external resistor connected between the ADD pin and AGND. Reference Table 6 for standard resistance values and their corresponding 7-bit address configurations.

Table 6. PMBus Address Settings and Resistor Values

ADDR1	ADDR2	ADDR3	ADDR4	1% Resistor (Ω)	Interleave Order
0x40	0x50	0x60	0x70	8200 (or connect the ADD pin directly to AGND)	4-bit, follow INTERLEAVE command, Interleave Order
0x41	0x51	0x61	0x71	13000	
0x42	0x52	0x62	0x72	20000	4-bit, follow INTERLEAVE command, Interleave Order
0x43	0x53	0x63	0x73	28000	
0x44	0x54	0x64	0x74	34800	4-bit, follow INTERLEAVE command, Interleave Order
0x45	0x55	0x65	0x75	43000	
0x46	0x56	0x66	0x76	52300	4-bit, follow INTERLEAVE command, Interleave Order
0x47	0x57	0x67	0x77	63400	
0x48	0x58	0x68	0x78	75000	4-bit, follow INTERLEAVE command, Interleave Order
0x49	0x59	0x69	0x79	86600	
0x4A	0x5A	0x6A	0x7A	100000	4-bit, follow INTERLEAVE command, Interleave Order
0x4B	0x5B	0x6B	0x7B	115000	
0x4C	0x5C	0x6C	0x7C	127000	4-bit, follow INTERLEAVE command, Interleave Order
0x4D	0x5D	0x6D	0x7D	143000	
0x4E	0x5E	0x6E	0x7E	164000	4-bit, follow INTERLEAVE command, Interleave Order
0x4F	0x5F	0x6F	0x7F	184000 (or connect the ADD pin directly to VDD)	

Analog Interleave Order Setting

The HP1000A supports initializing the interleave order based on the PMBus address detection result. 8 independent interleaved order settings for the address values are presented in Table 6. If the analog interleave order setting function is enabled, it forces rewriting the INTERLEAVE command setting using the PMBus address detection result.

LOW POWER MODE

The HP1000A can be turned off and enter Low-Power Mode either by activating the off state through the CTRL pin or by sending the OPERATION command. In Low-Power Mode, the ADCs are activated following a specific sequence at a very low frequency to reduce the power supply current to a extremely low level.

In this mode, the functional blocks of the HP1000A operate at a lower frequency, as summarized in Table 7. The device will exit Low-Power Mode and return to a unit-on condition when any of the following events occur, depending on the ON_OFF_CONFIGURATION setting: a signal via the CTRL pin, an OPERATION command, or the input voltage rising above the VIN_ON threshold.

Table 7 Operating Status of HP1000A Functional Blocks in Low-Power Mode

Blocks	Pins	Operating Status	Updating Frequency
Output Voltage Sense	VS+/VS-	Operation	1 s
Input Voltage Sense	VFF, VSET	Operation	Programmable, 8x/16x/32x/64x in 1 s
Input Current Sense	CS1	Disabled	/
Output Current Sense	CS2+, CS2-	Operation	1 s
IMON DAC	IMON	Disabled	/
Temperature Sense	TSNS/FLT	Operation	1 s
DOSA Trim	VSET	Disabled	/
Protections	/	Operation	Continues run
PWM	PWM1-6	Disabled	/
PMBus Interface	SDA/SCL	Operation	Continues run

DOSA TRIM

The trim input pin VSET is used to adjust the output voltage over the rated trim range. As illustrated in the trim equations and circuit diagrams below, trim adjustments use a single fixed resistor connected between the Trim input and VOUT Sense pin. Trimming resistors should have a low temperature coefficient (±100 ppm/deg.C or less) and be mounted close to the converter keeping leads short. If the trim function is not used, disable the analog trim function, the converter will default to its specified output voltage accuracy.

Trim equations (based on 12 V output) are expressed as follows:

$$R_{TRIM\_D} = \left(\frac{511}{\Delta\%}\right) - 10.22\ (k\Omega)$$

$$R_{TRIM\_U} = \left(\frac{5.11V_{OUT\_NOR}(100+\Delta\%)}{1.225\Delta\%}\right) - \frac{511}{\Delta\%} - 10.22\ (k\Omega)$$

Where,

$$\Delta\% = \frac{V_{OUT\_NOR} - V_{OUT\_TG}}{V_{OUT\_NOR}} \cdot 100\%$$

V_{OUT_NOR} is the nominal output voltage and V_{OUT_TG} is the target trimmed output voltage. Note that "Δ" is given as a small fraction, not a percentage.

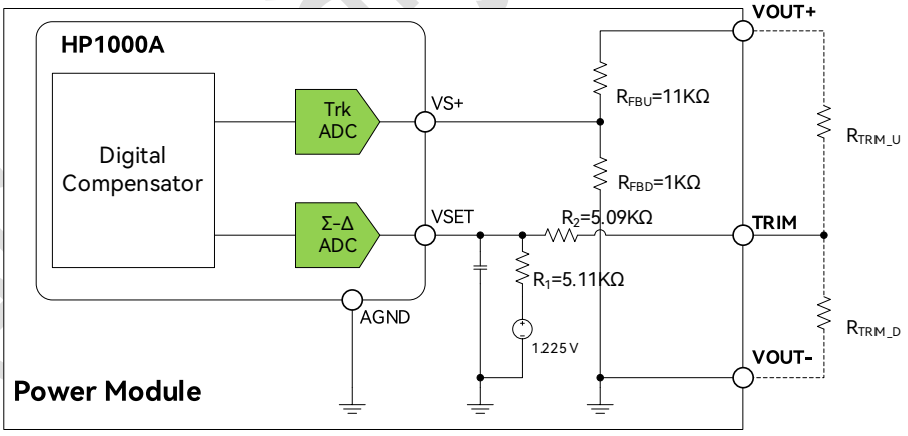


Figure 21 Diagram of DOSA Analog Trim

The VSET/ROV PIN is a multi-functional pin, and it will enable external reference for VOUT modulation when set as VSET. The VSET has an input range of 1.6 V and 12-bit resolution, which means LSB = 1.6 V / 4096 = 390.625 μV. The nominal reference voltage is based on 1.0 V on VS+/VS-, therefore, the trimmed voltage will refer to the nominal voltage as expressed,

$$V_{DOSA\_REF} = \frac{V_{SET}}{1.225V} \times \frac{1.225V}{1.0\text{V}} \times \frac{2560}{3136}$$

A internal digital gain adjustment for the user is set by VSET_GAIN_TRIM, which default value is 0.8163 with ±25% adjustable range, also a additional VSET_OFFSET_TRIM is supported. And the VSET sampling rate can be configured as 10.5 ms or 1.31 ms.

POWER MONITORING

The HP1000A integrates a comprehensive power monitor function, enabling real-time, high-precision system surveillance. This is achieved through its internally integrated ADC and PWM modules, which continuously monitor critical parameters including input voltage, output voltage, input current, output current, external temperature, duty cycle, switching frequency, and instantaneous output power.

The monitored data is accessible via standard PMBus commands such as READ_VIN and READ_IIN, providing a standardized digital interface for system communication and control. This digital power management capability delivers significant value for system monitoring.

FAULT RESPONSE AND FLAGS

The HP1000A has an extensive set of flags that are activated when certain limits, conditions, or thresholds are exceeded. Responses to these flags are individually programmable: They can be ignored or configured to trigger actions such as disabling specific PWM outputs, entering constant current mode, or even shutting down the power supply. Additionally, the HP1000A can be programmed to execute responses when these flags are reset.

The HP1000A also includes a set of latched fault registers. These registers mirror the flags reported by the PMBus STATUS_x commands (0x7A to 0x80), but with a key distinction: Flags in the latched registers remain persistently set to facilitate detection of intermittent faults. The CLEAR_FAULTS command (Command 0x03) serves to clear both the latched fault registers and reset all associated flags.

Table 7 provides a summary of faults and respective debounce types.

Table 7 Summary of Faults and Respective Responses Supported by HP1000A

Fault Type	Pin	Comments	Debounce	Response
VOUT_OV_FAST	VS+	VS+ internal connected to an analog comparator used as fast over-voltage protection.	Y	VOUT_OV_FAST_ RESPONSE
ROV_FAST	ROV	ROV analog comparator on this pin provides this protection as redundancy over-voltage protection when enabled.	Y	ROV_FAST_ RESPONSE
VOUT_OV	VS±	The ADC on these pins is averaged every 16 times with 11-bit accuracy for this fault. This information is compared with the VOUT_OV_FAULT_LIMIT to set the flag.	Y	VOUT_OV_FAULT_R ESPONSE
VOUT_OV_WARN	VS±	Same as VOUT_OV.	N/A	N/A
VOUT_UV_WARN	VS±	Same as VOUT_UV.	N/A	N/A
VOUT_UV	VS±	The ADC on these pins is averaged every 16 times with 11-bit accuracy for this fault. This value is compared with the VOUT_UV_FAULT_LIMIT to set the flag.	Y	VOUT_UV_FAULT_R ESPONSE
IOUT_OC	CS2±	The ADC on these pins is averaged every 163.84 µs with 12-bit accuracy for this fault. This value is compared with the IOUT_OC_FAULT_LIMIT to set the flag.	Y	IOUT_OC_ FAULT_RESPONSE
IOUT_OC_LV	VS±	The ADC on these pins is averaged every 16 times with 11-bit accuracy for this fault. This value is compared with the IOUT_OCLV_FAULT_LIMIT to set the flag when the fault response type of IOUT_OC_FAULT_RESPONSE is set as 0x1.	Y	IOUT_OC_LV_FAULT _RESPONSE
ISHARE	IMON	The output of current sharing loop is exceeding limits.	Y	ISHARE_FAULT_RE SPONSE

IOUT_OC_FAST	CS2±	An analog comparator on this pin provides this protection.	Y	IOUT_OC_FAST_FAULT_RESPONSE
IOUT_UC	CS2±	The ADC on this pin is averaged every 0.655 ms with 12-bit accuracy for this fault. This information is compared with IOUT_UC_FAULT_LIMIT to set the flag.	Y	IOUT_UC_FAULT_RESPONSE
IOUT_UC_FAST	CS2±	An analog comparator on this pin provides this protection.	Y	IOUT_UC_FAST_FAULT_RESPONSE
IIN_OC	CS1	The ADC on this pin is averaged every 0.655 ms with 12-bit accuracy for this fault. This information is compared with the IOUT_OC_FAULT_LIMIT to set the flag.	Y	IIN_OC_FAULT_RESPONSE
IIN_OC_FAST	CS1	An analog comparator on this pin provides this protection.	Y	IIN_OC_FAST_FAULT_RESPONSE
IOUT_OC_WARN	CS2±	Same as IOUT_OC.	N	N/A
VIN_UV	VFF	The ADC on this pin is averaged every 16x times with 11-bit accuracy for this fault. This information is compared with the VIN_UV_FAULT_LIMIT to set the flag.	Y	VIN_UV_FAULT_RESPONSE
VIN_UV_WARN	VFF	Same as VIN_UV.	N	N/A
VIN_OV	VFF	The ADC on this pin is averaged every 16x times with 11-bit accuracy for this fault. This information is compared with the VIN_OV_FAULT_LIMIT to set the flag.	Y	VIN_OV_FAULT_RESPONSE
VIN_OV_WARN	VFF	Same as VIN_OV.	N	N/A
POUT_OP	N/A	The multiplication of VS and CS2 ADCs averaged every 2.6 ms with 11-bit accuracy for this fault. This information is compared with the POUT_OP_FAULT_LIMIT to set the flag.	Y	POUT_OP_FAULT_RESPONSE
OT	TSNS	The ADC on this pin is averaged every 200 ms with 14-bit accuracy for this fault to provide reading (external NTC temperature sensors). This information is compared with the OT_FAULT_LIMIT to set the flag.	Y	OT_FAULT_RESPONSE
OT_WARN	TSNS	Same as OT.	N	N/A
GPIOx_FAULT	GPIOx	X = 1, 2, 3/4. External fault input detection.	Y	GPIOx_FAULT_RESPONSE
TSNS_FAULT	TSNS	TSNS/FLT detection for the type of DrMOS TSNS/FLT interface.	Y	TSNS_FAULT_RESPONSE
TON_MAX	N/A	The maximum time that the unit can attempt power up to the output without reaching the output under-voltage fault limit.	Y	TON_MAX_FAULT_RESPONSE
TOFF_MAX_WARN	N/A	The maximum time that the unit can attempt to power down the output without reaching 12.5% of the output voltage programmed at the time the unit is turned off.	N	N/A
VDD/VCORE_OV	VDD VCORE	VDD over-voltage fault.	Y	Ignore or Shutdown
VDD UV	VDD	VDD under voltage fault.	Y	Shutdown

CHIP PASSWORD

The User Password is a unique 32-bit code that is entered using the USR_PASSWD command. Because this command is a block read/block write command, the first data byte of this command is the number of 4 bytes. After the correct user password is entered, the user has full write access to all the user commands.

EEPROM

The HP1000A incorporates an EEPROM controller managing its embedded 512-byte memory with single-page architecture (containing both user-configurable parameters and factory-preset values). In default locked state during power-up/POR sequence, the EEPROM enforces triple protection: write-blocked, erase-disabled, and full-array read-prohibited. A security handshake protocol must be executed to unlock R/W/E privileges, which remain active until system reset triggers auto-relock. Notably, the EEPROM power rail automatically deactivates when accessing configuration data post-POR, requiring manual power re-initialization via PMBus interface before executing critical operations (STORE_USER_ALL programming or RESTORE_USER_ALL restoration), ensuring fail-safe configuration management.

PMBUS INTERFACE

The PMBus slave interface facilitates communication with PMBus-compliant master devices, conforming to the PMBus Power System Management Protocol Specification (Revision 1.2) . This 2-wire interface supports multi-master and multi-slave bus configurations and is compatible with master devices regardless of Packet Error Checking (PEC) support. The following features are supported by HP1000A,

- Slave operation on multiple device systems
- 7-bit PMBus addressing with programmable base address
- Normal mode (100 kbps) and Fast mode (400 kbps) data transfer rate
- Support PEC (Packet error check)
- Support clock stretching
- Support Group Command Protocol
- Support Alert Response Address Protocol with arbitration
- Support General Call address

Transfer Protocol

The PMBus slave interface implements the transfer protocol defined in the System Management Bus (SMBus) Specification, Version 2.0. Diagrams of SMBus transaction data structures as they appear on the bus are of the form,

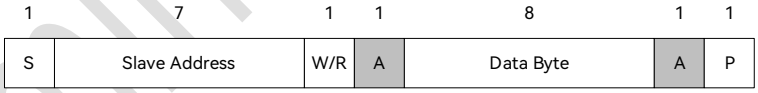


Figure 22 General Transaction Diagram

Table 8 SMBus Packet Protocol Diagram Element Key

Symbol	Meaning
S	The START condition sent from a bus master device
Sr	A REPEATED START condition sent from a bus master device
A	An Acknowledge (ACK) condition sent from the master device
A	An Acknowledge (ACK) condition sent from the slave device
NA	A Not Acknowledge (NACK) condition sent from the master device
NA	A Not Acknowledge (NACK) condition sent from the slave device

P	A STOP condition sends by a bus master device
R	The bit [0] of the address byte with a value of 1, indicating the device is being addressed with a read
W	The bit [0] of the address byte with a value of 0, indicating the device is being addressed with a write
	Data transaction from slave device to mast device
	Data transaction from master device to slave device

Extended Commands

The Extended Command protocol enables an additional 256 command codes by utilizing a two-byte command structure. The first byte (the least significant byte, or LSB) is a reserved value that signals the use of the extended command format. The second byte (the most significant byte, or MSB) contains the actual command to be executed. The protocol details for single-byte read or write operations are illustrated below.

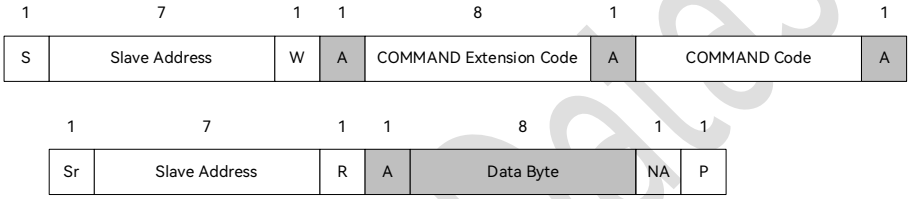


Figure 23 Extended Command Read Byte Protocol

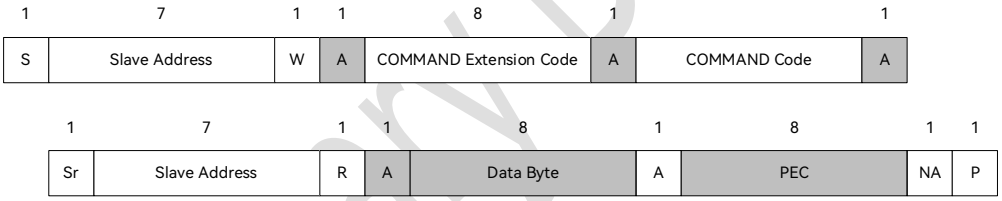


Figure 24 Extended Command Read Byte Protocol With PEC

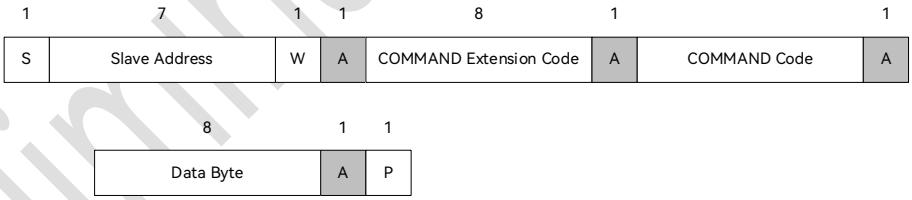


Figure 25 Extended Command Write Byte Protocol

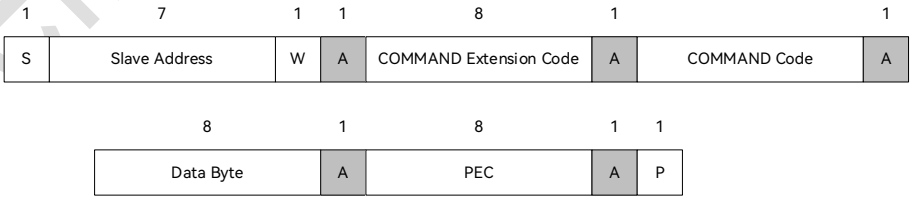


Figure 26 Extended Command Write Byte Protocol With PEC

The details of the protocol for commands that read or write one word are illustrated below.

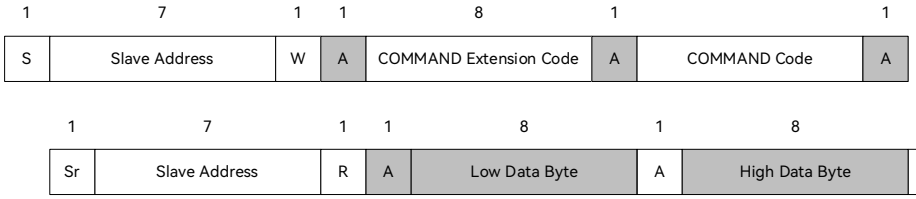


Figure 27 Extended Command Read Word Protocol

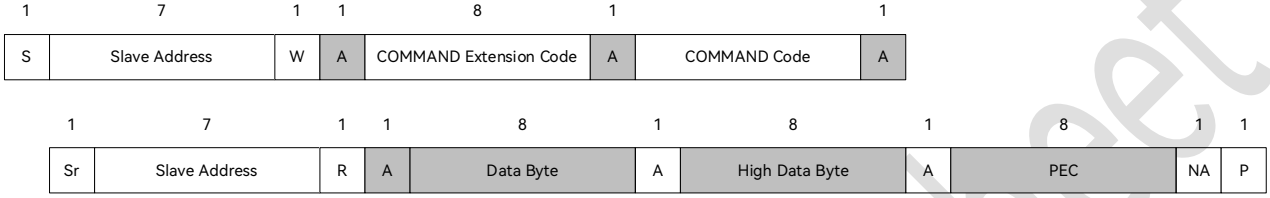


Figure 28 Extended Command Read Word Protocol With PEC

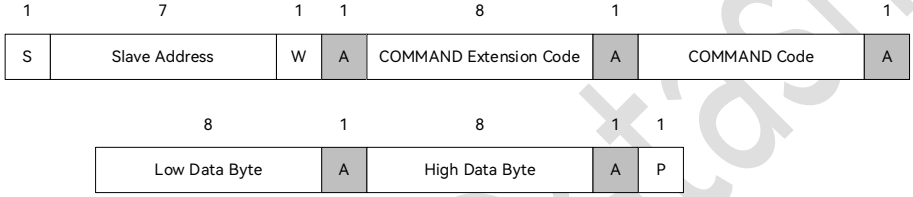


Figure 29 Extended Command Write Word Protocol

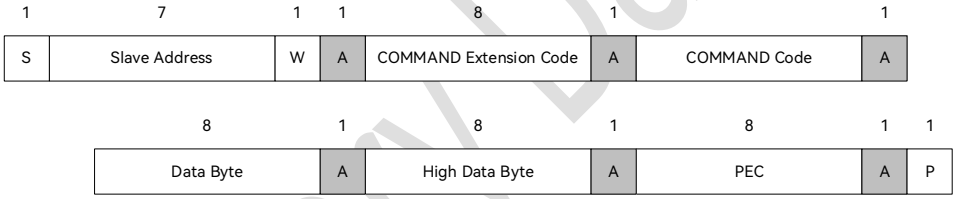


Figure 30 Extended Command Write Word Protocol With PEC

Packet Error Checking

The PMBus controller incorporates Packet Error Checking (PEC) to enhance communication reliability and data integrity. This feature is implemented by appending a PEC byte at the end of each message transaction.

The PEC byte is generated using a CRC-8 (Cyclic Redundancy Check) algorithm. The calculation encompasses all bytes transmitted in the transaction, including the slave address (with Read/Write bit), command code, and data bytes, from the start condition to the stop condition. Notably, protocol control bits such as Start, Restart, Acknowledge (ACK), Not Acknowledge (NACK), and Stop are excluded from the PEC calculation.

The device that transmits the final data byte in the transaction is responsible for appending the calculated PEC byte. The receiving device must independently compute the PEC code using the same algorithm and compare it with the received byte to validate the transaction.

The PEC code is computed using the standard CRC-8 polynomial $C(x) = x^8 + x^2 + x^1 + 1$ (0b100000111). The hardware calculates the code sequentially, processing one byte at a time in order of transmission.

In a read transaction, the PMBus slave device calculates and appends the PEC byte immediately following the last data byte it sends to the master. In a write transaction, the PMBus slave device calculates the PEC code internally based on the received address, command, and data bytes. It then compares this internally generated code with the PEC byte sent by the master to verify the command's integrity before execution.

GUI SOFTWARE

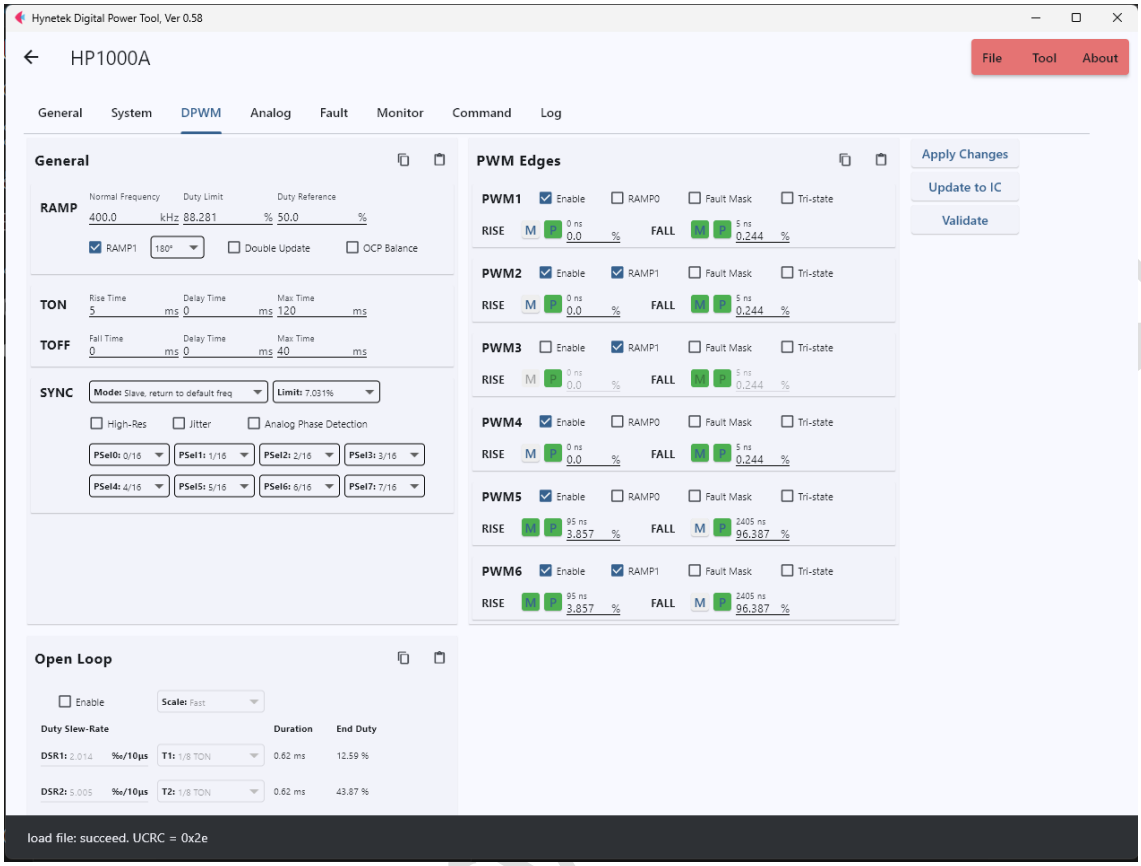


Figure 31 Using HP1000A GUI to Configure ON/OFF Timming and PWMs

A free, intuitive GUI is available for programming and configuring the HP1000A, specifically designed for power supply designers. This software dramatically reduces power supply design and development time.

TYPICAL APPLICATION CIRCUITS

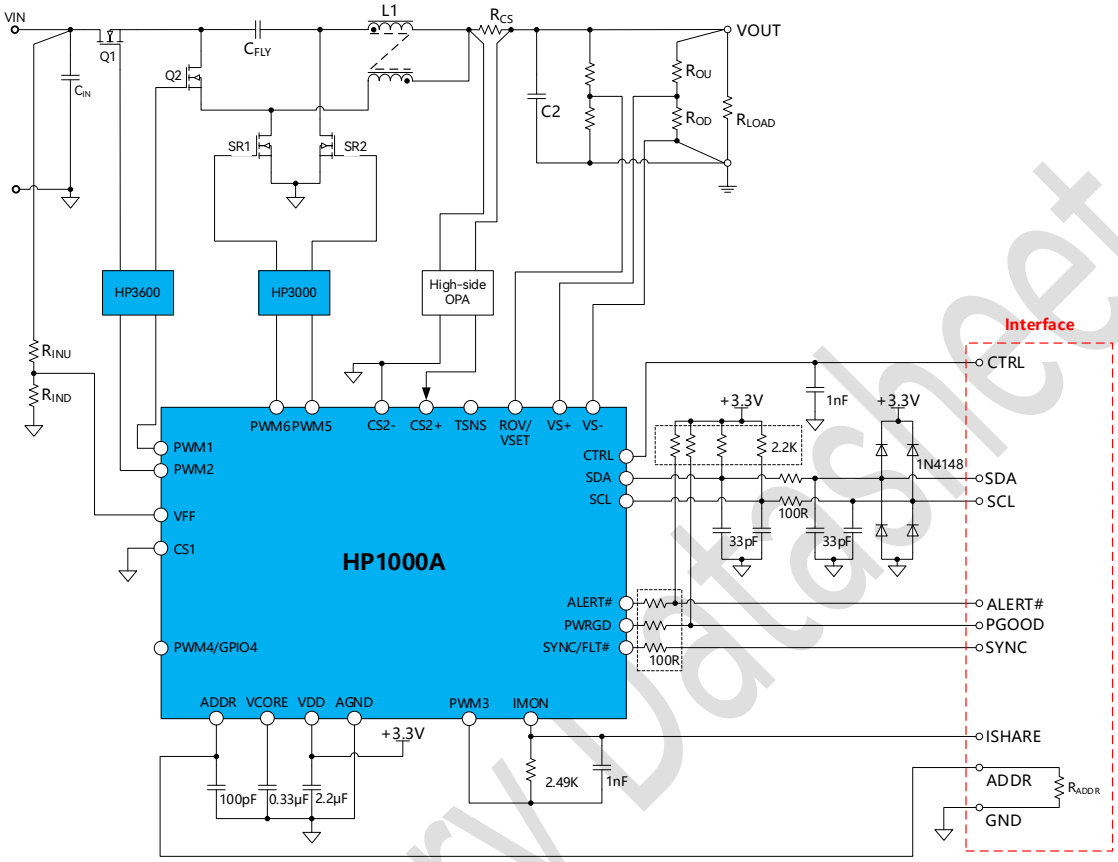


Figure 32. Typical Application Circuits of Switch-cap Converter

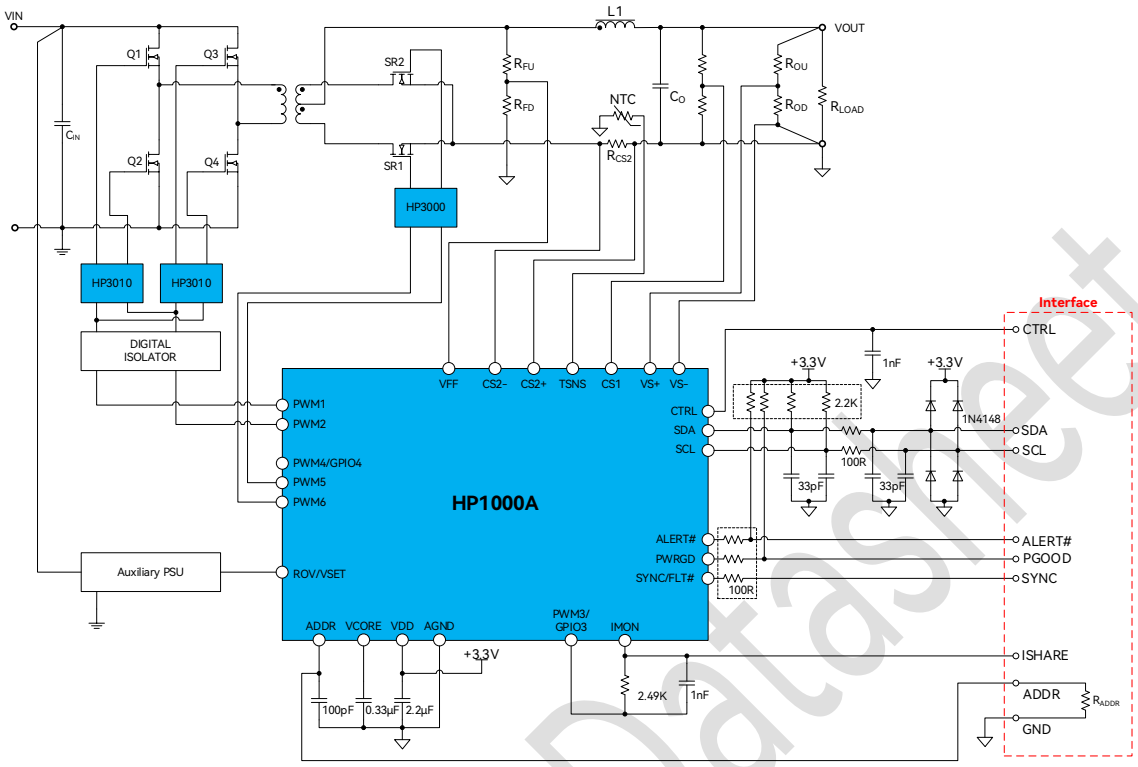


Figure 33. Typical Application Circuit of Hard-switching Full-bridge Converter

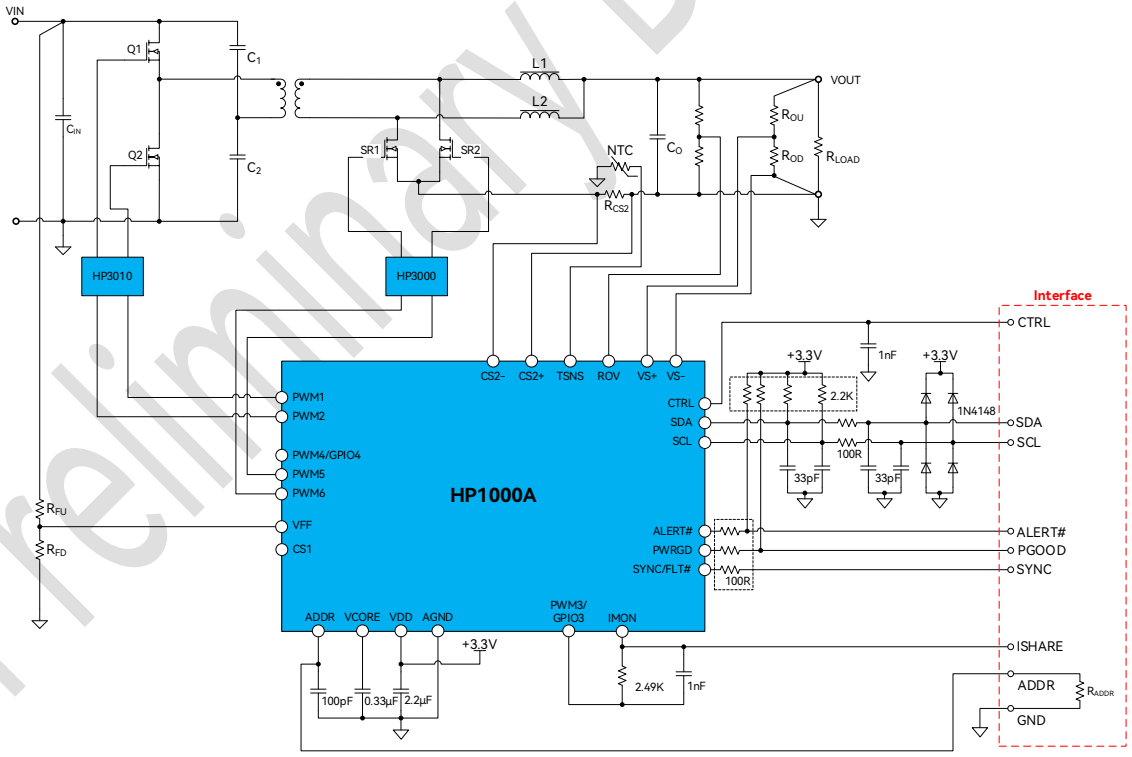
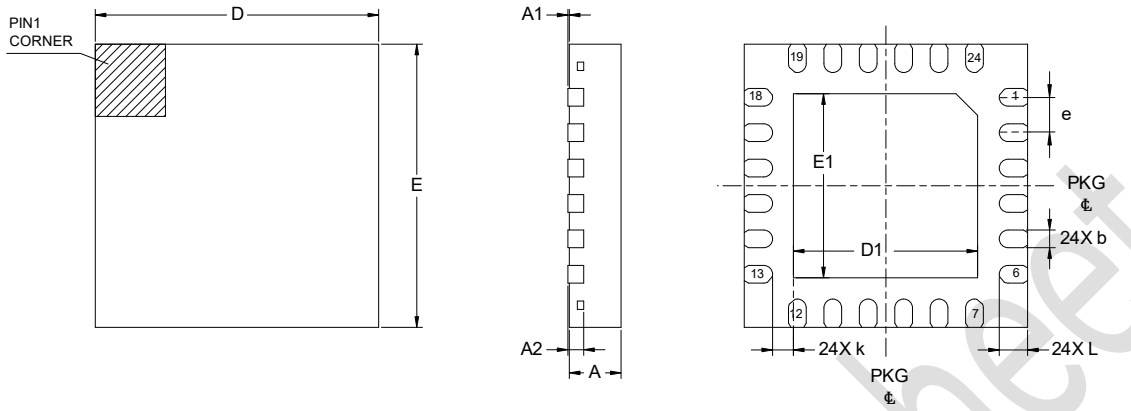


Figure 34. Typical Application Circuit of Non-isolated Half-bridge Current Doubler

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.40	2.70	2.80
E1	2.40	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN	

Figure 35. QFN-24L Package Outline Dimensions

PACKAGE TOP MARKING

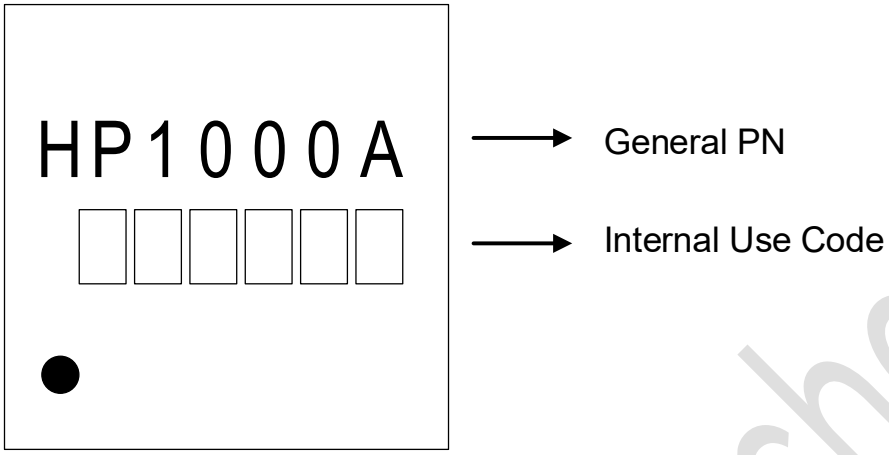


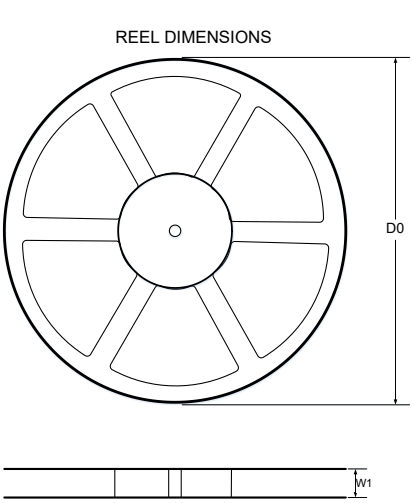
Figure 36. HP1000A-AA001-QN24R Package Top Marking

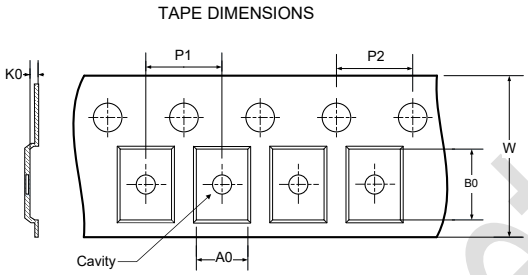
ORDERING GUIDE

Table 9.

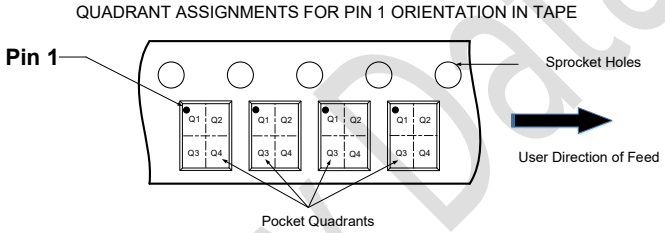
Model	Temperature Range	Package Type	MSL	Package Option	Quantity
HP1000A-AA001-QN24R	-40°C to +125°C	QFN-24L	3	T&R	5000

TAPE AND REEL INFORMATION





A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP1000A-AAXXX-QN24R	QFN-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Figure 37. Tape and Reel Information

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